REVISION HISTORY

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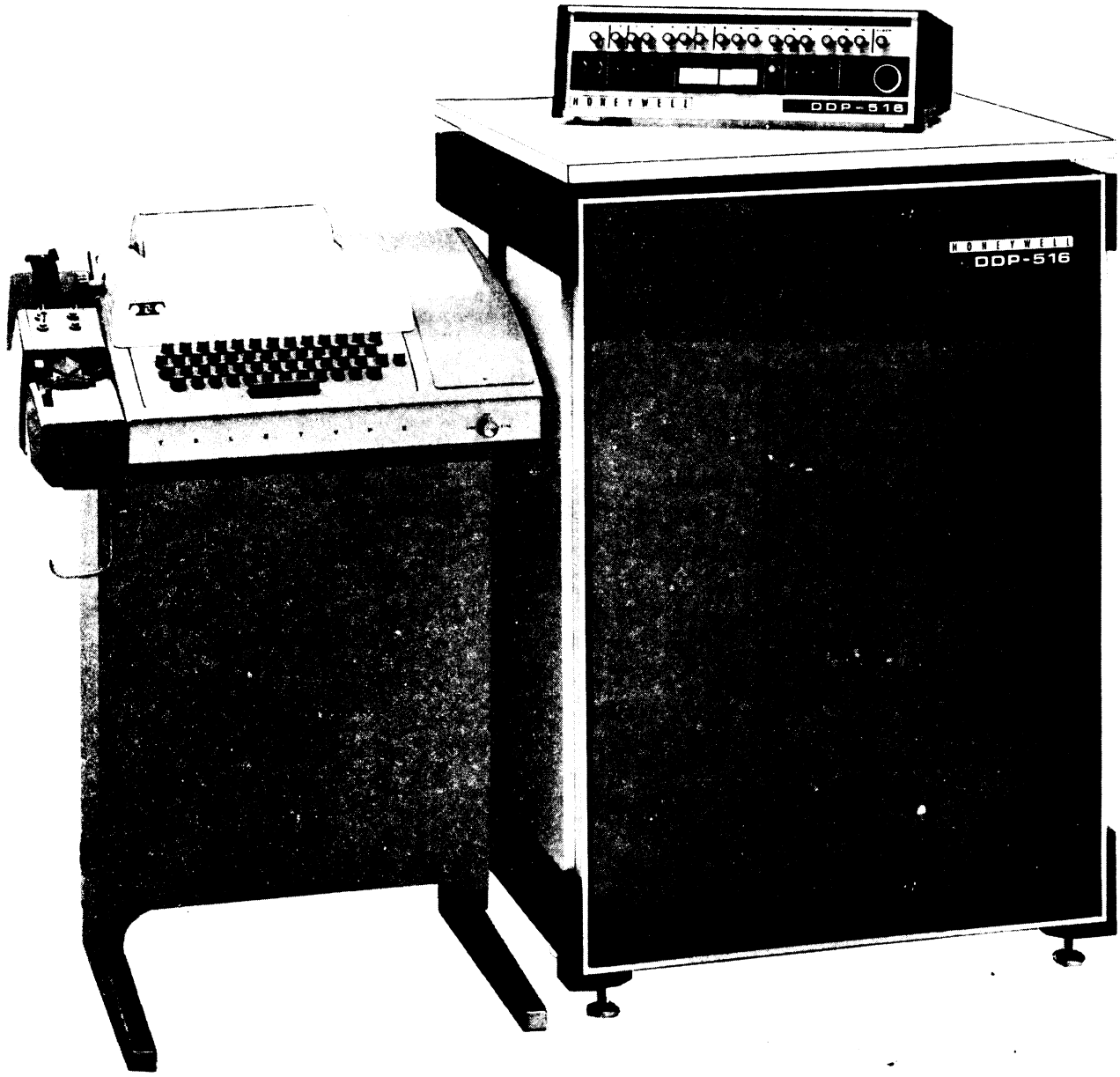

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DDP-516 General Purpose Computer

INTRODUCTION

The DDP-516 is an integrated circuit 16-bit binary word general purpose digital computer with a 0.96 μsec cycle time magnetic core memory. The DDP-516 has a fully parallel machine organization and both indexing and multilevel indirect addressing. Memory sizes available are 4096, 8192, 12,228, 16,384, 24,576, and 32,768 words. Standard features include a flexible instruction repertoire of 72 commands, a hardware index register, a powerful I/O bus structure, and standard teleprinter keyboard and paper tape I/O unit. Options include memory parity, a high-speed arithmetic option, memory lockout, priority interrupt, a direct multiplex control unit, direct memory access, a real-time clock, and a full line of peripheral equipment.

The 16-bit word of the DDP-516 allows a straightforward and efficient addressing scheme. Most internal operations can be performed in two cycle times (1.92 μsec), or less including instruction access and execution time. A single word instruction can directly address any one of 1024 words. The 16-bit word is directly compatible with the ASCII 8-bit character code.

The DDP-516 is designed for both open-shop scientific applications and real-time on-line data processing and control. Modular design, a flexible I/O structure, and command repertoire enable the DDP-516 to be tailored to a broad variety of applications both on and off line. These include data reduction, process control, instrumentation, simulation and open-shop scientific and engineering computation.

Programming the DDP-516 computer is similar to programming other single-address binary computers using two's complement notation. Therefore, no major differences confront the programmer who is new to the DDP-516.

SECTION I
COMPUTER ORGANIZATION

SPECIFICATIONS

Type

Parallel binary

Addressing

Single address with indexing and indirect addressing

Word Length

16 bits

Machine Code

Two's complement

Memory Type

Magnetic core

Memory Size

4,096, 8,192, 12,288, 16,384, 24,576 or 32,768

Memory Cycle Time

0.96 μsec

Speed

Add: 1.92 μsec

Subtract: 1.92 μsec

Multiply (hardware option): 5.28 μsec max

Divide (hardware option): 10.56 μsec max

Standard Peripheral Equipment

ASR-33 or 35 Teletype Unit providing the following capabilities:

a. Read paper tape at 10 cps
b. Punch paper tape at 10 cps
c. Type at 10 cps
d. Keyboard input
e. Off-line paper-tape preparation, reproduction and listing

Optional Peripheral Equipment

300 cps photoelectric paper-tape reader

110 cps paper-tape punch

300 line-per-minute (120-character-per-line) high-speed printer

200 card-per-minute card reader

Magnetic tape units:

Unit	Tape Speed (ips)	Density (bpi)
Low speed	36	200, 556, 800
High speed	80	200, 556, 800

Standard Input/Output Lines

16-bit input bus

16-bit output bus

10-bit device address bus

External control and sense lines

Input/Output Modes

Three modes are available for data transfer between peripheral devices and the DDP-516.

a. Single word transfer with or without interrupt
b. Direct multiplex control (DMC) (optional)
c. Direct memory access (DMA) (optional)

Interrupt

Single interrupt line standard. Up to 48 optional priority interrupts are available.

Power Failure Protection

Power failure interrupt standard. Core memory protected against loss of information on ac power failure.

SYSTEM DESCRIPTION

Figure 1-1, a block diagram of the computer, shows the data storage registers, the control unit of the central processor and the input/output controls. The random access memory, shown as a single block, is a magnetic core unit containing one or more memory modules of 4096 or 8192 16-bit words. Data from the memory is transferred to and from the DDP-516 registers through the M-register. The functional units of the central processor and the input/output controls are as follows:

A-Register (A): A 16-bit register used as the primary arithmetic and logic register of the computer.

B-Register (B): A 16-bit secondary arithmetic register used primarily to hold arithmetic operands which exceed one word in length.

Program Counter (P): A 16-bit register that contains the location of the next instruction to be executed.

Adder: Performs the basic arithmetic processes of addition and subtraction.

M-Register (M): A 16-bit register used to transfer information to and from the magnetic core memory.

Y-Register (Y): A 16-bit register used to store the address for the memory.

C-Bit (C): A 1-bit indicator associated with the A- and B-registers, which stores overflow status resulting from the execution of arithmetic instructions, and stores the last bit shifted out of the A- or B-register during the execution of shift instructions.

Index Register (X): A 16-bit register used for address modification. Any memory write cycle addressing memory location zero also loads the X-register.

Output Bus (OTB): Sixteen lines that transmit data from the computer A-register to an I/O device.

Input Bus (INB): Sixteen lines that transmit data from an I/O device to the computer A-register.

Address Bus (ADB): Ten lines used in conjunction with I/O devices. Bits on lines 7 through 10 define the function to be performed by the I/O device. Bits on lines 11 through 16 designate the I/O device to be used.

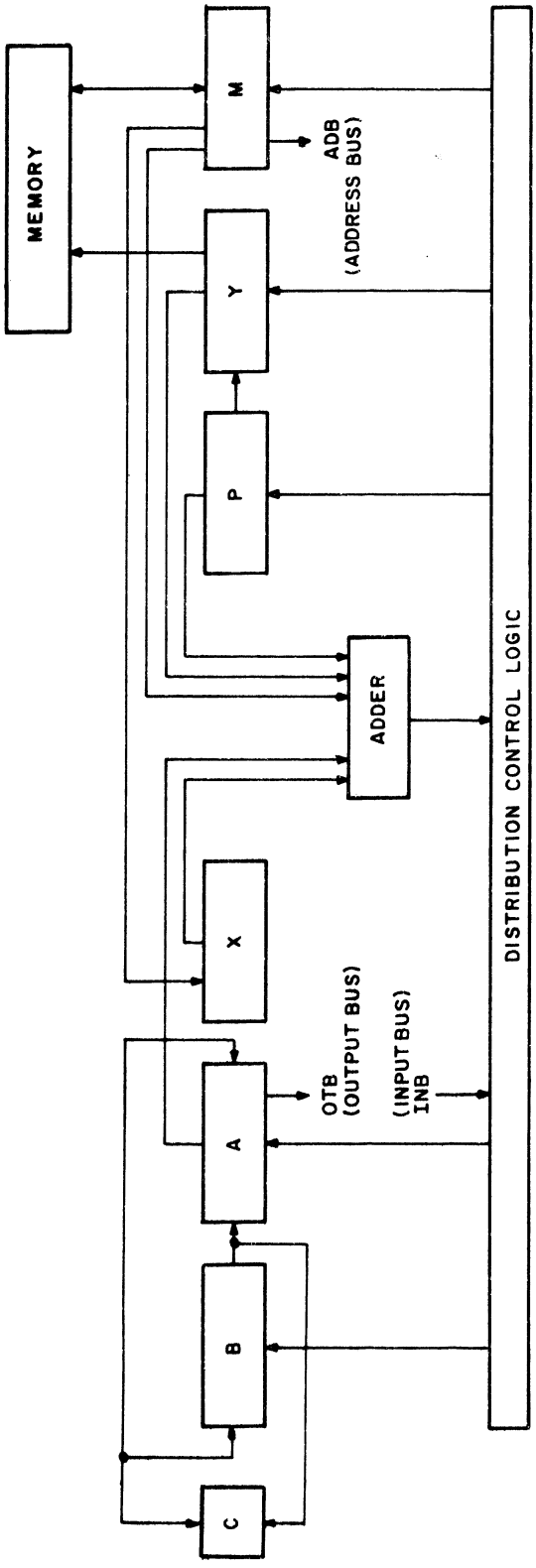


Figure 1-1. DDP-516 Simplified Block Diagram

WORD FORMATS

Data Formats

Single Precision. -- The format for data words stored in the computer is shown in Figure 1-2.

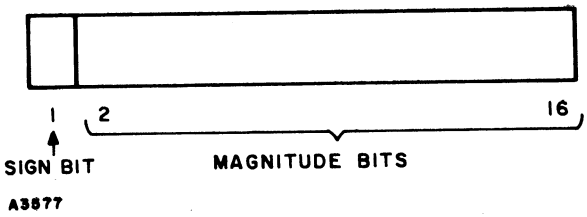


Figure 1-2. Data Word Format, Single Precision

Sixteen-bit data words are stored in two's complement form. The first bit of a data word may be considered the arithmetic sign and is zero for positive data.

Double Precision. -- When greater precision is required than that obtainable when using the single precision format, the double precision format is used (Figure 1-3). The sign position of the second (least significant) word is always zero. Thirty bits of magnitude are obtainable. This is the format for the product of the multiplication of two single precision words. It is also the data format for double precision operations.

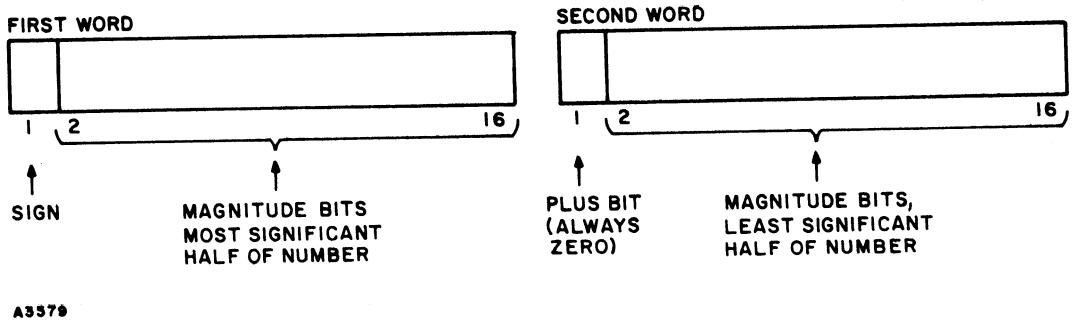


Figure 1-3. Data Word Format, Double Precision

Logical Data. -- Logical data, such as the condition of sixteen binary indicators, can be stored in a single data word. This type of data is generally not treated arithmetically by the program but logically by means of Boolean operators such as "AND" and "exclusive OR." In this case, bit 1 of a word does not represent the sign but the first of sixteen conditions.

Instruction Words. -- Instruction words are divided into four types: memory reference, input-output, shift, and generic.

The basic instruction word format in the computer is that for a memory reference instruction, which is shown in Figure 1-4. Bits 3 to 6 contain the operation code, which defines the function to be performed. For example, if bits 3 to 6 contain 0110 $(06)_8$ the instruction is identified as an add instruction; if they contain 1001 $(11)_8$ the instruction is a compare. For ease of communication, operation codes are generally expressed either in octal or as a mnemonic. "Subtract," for example, which has an op-code bit configuration of 0111, is referenced in machine language as $(07)_8$ and has a mnemonic of SUB. The latter is the way the programmer writes an op code when programming in DAP 16, the computer's assembly language.

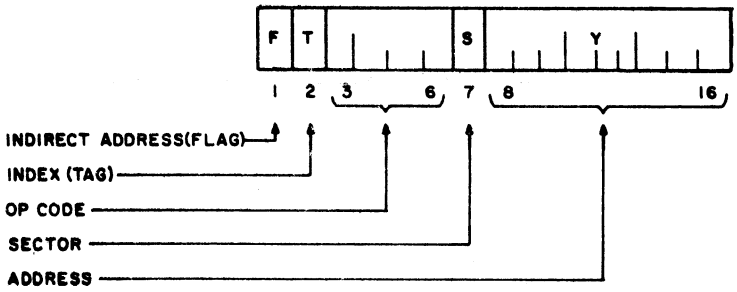


Figure 1-4. Memory Reference Instruction Format

The input/output instruction word format is shown in Figure 1-5. Bits 1 through 6 specify the particular I/O instruction; bits 11 through 16 specify which device is being addressed. Bits 7 through 10 define the function to be performed by the instruction.

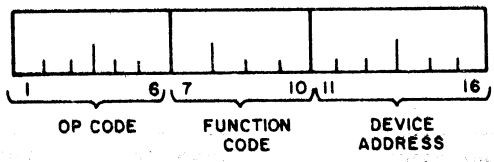


Figure 1-5. Input/Output Instruction Format

The shift instruction word format is shown in Figure 1-6. Bits 1 through 10 specify the type of shift; and bits 11 through 16 are used to define the number of shifts to be performed. The number of shifts must be represented in two's complement form.

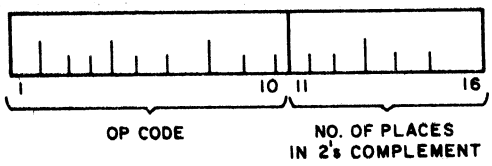


Figure 1-6. Shift Instruction Format

MEMORY ADDRESSING

A memory reference instruction (see Figure 1-4) can utilize several techniques for addressing memory: direct addressing, indexing, and indirect addressing. Indexing and indirect addressing may be specified in the same instruction, and indexing may be pre- or post-indirect addressing. Multilevel indirect addressing is provided.

Direct Addressing

The memory of the DDP-516 is considered to be divided into sectors of 512 words each (i.e., a 4096-word computer will have eight sectors). Any word in a sector can be addressed with nine bits ($2^9 = 512$). The address portion of a memory reference instruction (bits 8 to 16) can thus define a unique word in a sector. Addresses within sectors run from $(000)_8$ to $(777)_8$. The sector bit, bit 7 of the instruction, identifies the sector of the word addressed in accordance with the following rules:

Sector Bit = 0 The address is in sector 0 (octal address 0000 - 00777).

Sector Bit = 1 The address is in the same sector as the instruction being executed.

For example, assume an ADD instruction having an address of 444 is in location $(02100)_8$, or sector 2 word 100. If the sector bit in the instruction is 0, the instruction references word 444 in sector 0, or $(00444)_8$. If the sector bit is 1, then the instruction references word 444 in sector 2, or $(02444)_8$, because the instruction itself is in sector 2.

A single instruction can thus directly address 1024 words, half of which are in sector 0 and half of which are determined by the location of the instruction. Figure 1-7 represents the memory that can be directly addressed by an instruction in sector 2 and an instruction in sector 6.

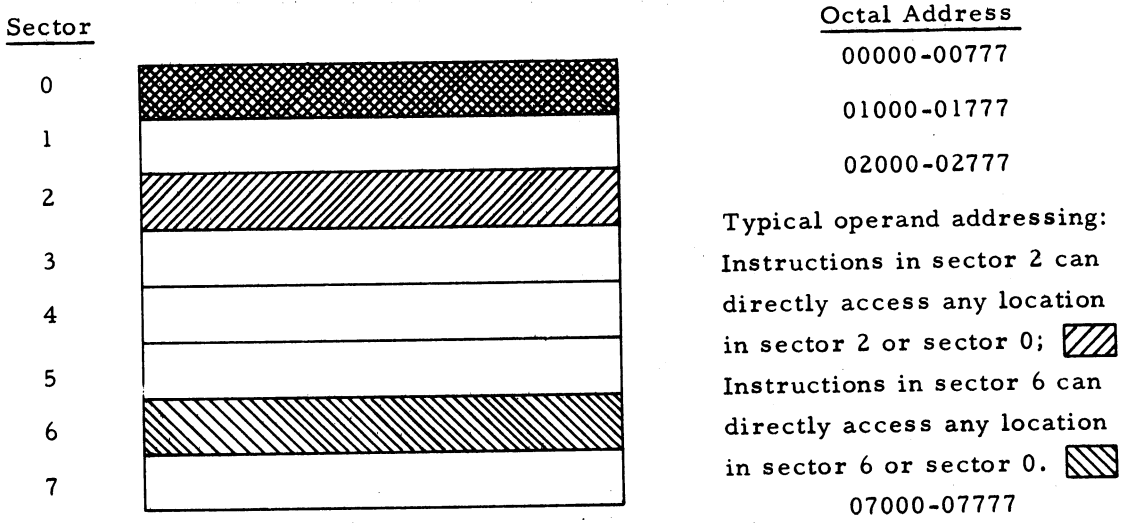


Figure 1-7. Memory Sectors in 4096-Word DDP-516

Indexing

The index register is a 16-bit hardware register whose contents can be added to the direct address of an instruction to produce a new effective operand address. This action causes no increase in instruction execution time. Indexing is specified by putting a ONE in bit 2 of a memory reference instruction.

If indexing is specified, the value in the index register is added algebraically to the direct address. The index register can contain either a positive or negative (two's complement) value, although negative values are generally utilized.

For example, if the index register contained -2, $(177776)_8$, and the ADD 444 instruction at $(02100)_8$ mentioned in the previous section were executed with both the index and sector bits set, the effective address would be $(02444)_8 + (177776)_8$ or $(02442)_8$. Note that sector boundaries can be crossed with no increase in instruction execution time.

The index register can be loaded or stored directly by means of the load index (LDX) and store index (STX) instructions. In addition, any instruction that addresses memory location 0 addresses the index register. The usual way of incrementing the index register is by an IRS 0 instruction.

Indirect Addressing

If bit 1 of a memory reference instruction is set, indirect addressing takes place. When indirect addressing is specified, the effective address of the operand is assumed to be the content of the location specified by the direct address. The format of the indirect address location is shown in Figure 1-8.

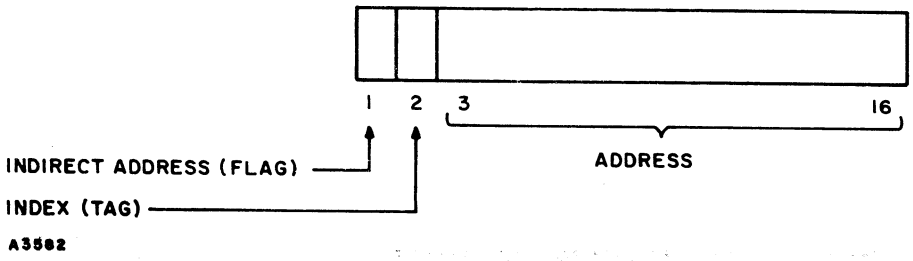


Figure 1-8. Indirect Address Format

To illustrate indirect addressing, consider that an add command in sector 2 is flagged for indirect addressing (this is specified in DAP by placing an asterisk after the op code).

```
ADD*      444
```

Location 444 contains

$(06231)_8$

The effective address would then be $(06231)_8$, which is in sector 6. The content of location 06231 would be added to the A-register

Since the address field in the indirect address location is 14 bits, up to 16K of memory can be addressed in this mode. Indirect addressing adds a cycle to the execution time of an instruction.

Multi-Level Indirect Addressing

Bit one of the indirect address work also contains a flag bit. If this is set, another level of indirect addressing occurs. This chaining of indirect addressing will continue until an indirect address word is reached whose flag bit is zero. Each level of indirect addressing adds a cycle to instruction execution time.

NOTE

With the memory lockout option (page 4-9), instructions executed in the restricted mode cause an interrupt if more than 8 levels of indirect addressing are attempted.

Indirect, Pre-Index

Pre-indexing occurs if both the indirect and index bits of an instruction are set. In this case, indexing is applied to the direct address to determine the location of the indirect address.

Indirect, Post-Index

If the indirect bit in an instruction is set, and if the index bit is set in the indirect location as opposed to the instruction itself, indexing is applied to the indirect address to determine the location of the operand. This action is called post-indexing.

Addressing Summary

Figure 1-9 is a flow-chart which shows the various phases in developing the effective address of a memory reference instruction. It is for the normal mode only and does not cover the development of addresses in the following cases:

a. Memory lockout is included in the system and the base (J) register is not zero. (See page 4-9.)

b. The system contains more than 16K of memory and the extend mode is being utilized. (See page 4-1.)

Locations $(00001)_8$ to $(00017)_8$

Memory locations $(00001)_8$ through $(00017)_8$ are protected in the standard machine against being written into under program control. Information may be read from these locations in the normal manner, however, all instructions which attempt to write in them will be aborted. The only way in which these locations may be loaded is through the use of

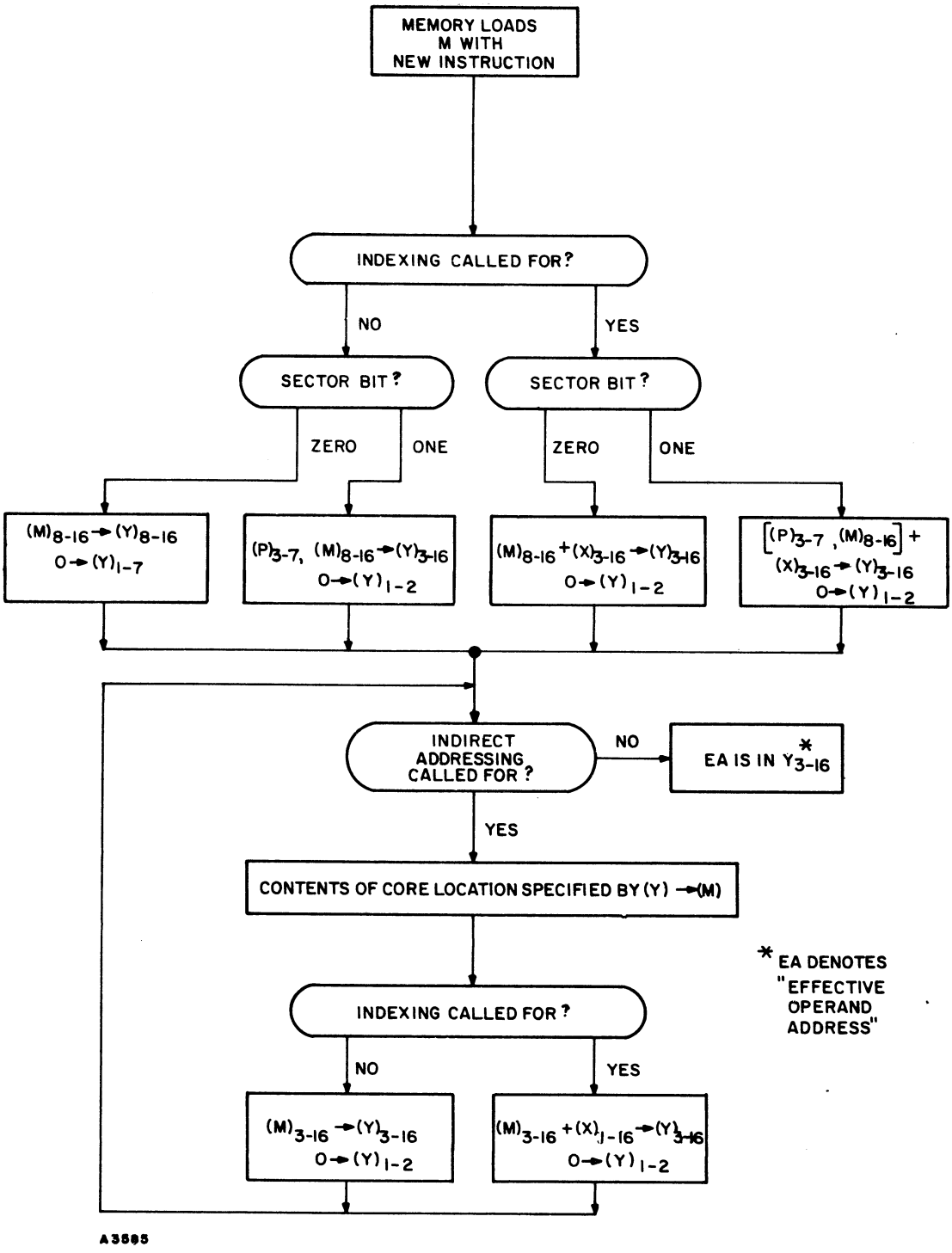


Figure 1-9. Fetch, Indexing and Indirect Addressing, Logic Flow Diagram

of the memory access feature of the console (see Section VI). The locations provide protected storage for the Key-In Loader utilized with the software system. See Appendix H.

Location $(00000)_8$ (Index Register)

The hardware index register tracks the dedicated memory location $(00000)_8$ (index register), that is, any modification of location $(00000)_8$ will cause the hardware index register to be changed to agree with $(00000)_8$. For systems with memory lockout see Section IV.

Instruction Sequence

Programs are executed sequentially with the contents of the program counter (P-register) being incremented by one upon the execution of each instruction. Certain instructions (Skips, Compare, I/O) conditionally increment the program counter by an additional one or two, thereby causing a skip. Others (Jump, Jump-Store) unconditionally load the program counter with the effective address, thereby causing a branch in the program.

Breaks

Certain operations may occur between instructions or between cycles of instructions without effecting the contents of the program counter. When the operations are complete, the program resumes. These actions are called "breaks", and include such operations as DMA or DMC I/O cycles, incrementation of the real time clock, and memory increment breaks.

Interrupts

An interrupt is different from a break in that an action occurring independently of a program can cause the contents of the program counter to be automatically changed, thereby changing the sequence of instruction execution. Interrupts have unique memory locations dedicated to them, whose contents are interpreted as an indirect address. The action of an interrupt causes the program to branch to the location whose address is stored in the dedicated location.

Interrupts are caused by the following:

I/O Interrupts
Power Failure Interrupt
Memory Lockout Interrupts
Additional Interrupts

Memory Access Priority Structure

The various functions that the computer performs are executed in a priority sequence if two or more functions are trying to simultaneously access memory. The following chart shows the relative priorities between the program and breaks and interrupts. Details on the latter are explained in the following chapters.

Table 1-1.
DDP-516 Computer Access-to-Memory Priority Structure

Relative Priority Level	Option/Function
1	Direct Memory Access Break (DMA) 516-21
2	Direct Multiplex Control Break (DMC) 516-20
3	Power Failure Interrupt (PFI), Standard
4	Real Time Clock Break 516-12
5	Memory Lockout Violation Interrupt 516-08
6	Standard Interrupt Standard
7	Memory Increment Break 516-26
8	Priority Interrupt 516-25
9	Central Processing Unit (CPU)

SECTION II
STANDARD INSTRUCTIONS

INSTRUCTION REPERTOIRE

The instructions which comprise the standard DDP-516 Instruction Repertoire are described in detail in this section. Mnemonics and symbols used in the instruction descriptions are listed in Table 2-1. A thorough knowledge of the data presented in Table 2-1 is necessary to understand the instruction descriptions.

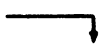
Table 2-2 lists all standard instructions. Each instruction is identified by its assigned three-letter mnemonic, type symbol, and octal Op-Code. Definitions, descriptions, and timing data for each instruction are also included in Table 2-2. Refer to Section I for instruction word formats.

The standard instructions in Table 2-2 are grouped into the following operational categories:

Load and Store
Arithmetic
Logical
Shift
Input/Output
Control
Half-Word

Arithmetic instructions which provide overflow detection are indicated by the designation Overflow Status → (C). If overflow occurs on a particular instruction, the C-bit is set to a one. If overflow does not occur, the C-bit is reset to a zero. Thus, after each arithmetic instruction, the contents of the C-bit indicates whether or not overflow occurred on that instruction.

Table 2-1.
Glossary of Symbols

Symbol	Definition
EA	Effective operand address; the address from which the operand will be obtained. This is determined only after all selection of sectors, indexing, and indirect addressing have been performed.
n	Specified number of shifts to be performed.
N	Two's complement of the number of shifts to be performed.
ADB	Address Bus
INB	Input Bus
OTB	Output Bus
EXTMD	Extended Mode Indicator - associated with Extended Addressing Model 516-05, 06
DP Mode	Double Precision Mode associated with Model 516-11
A	A-Register (16-bits)
P	Program Counter (16-bits) -
B	B-Register (16-bits)
E	E-Register (16-bits)
X	Index Register (16-bits)
M	M-Register (16 bits)
C	C-bit (1 bit)
	Replaces
	Is exchanged with
	Is discarded
	Logical AND
	Logical OR
	Exclusive OR
+	Algebraic Addition
( )	Contents of a hardware register (e. g., (A) = contents of A-Register)
[ ]	Contents of core location specified by (e. g. [EA] = contents of core location specified by EA)
T	Tag Bit (bit 2 of instruction word)
MR	Memory Reference Instruction
G	Generic Instruction
SH	Shift Instruction
IO	Input-Output Instruction

SECTION III
INPUT/OUTPUT
AND
STANDARD INTERRUPTS

INPUT/OUTPUT CONTROL AND COMMUNICATION

The basic input/output system of the DDP-516 consists of an I/O bus to which are interfaced various devices. A "device" may be a peripheral unit such as a paper tape reader, a magnetic tape control unit with several transports, or an analog-digital subsystem with dozens of channels. Each device is unique in that it has a single interface, and as far as the computer is concerned, a single address. Up to 20 devices may be attached to the I/O bus.

Each device is individually buffered. Input/output transfers take place between the central processor and the buffer within the device interface via the I/O bus. All transfers are word parallel and are effected at microsecond speeds. Buffers in device interfaces may be up to 16-bits in length, although they are less for many character-oriented devices.

Device buffers are unloaded to or loaded from the device itself at the rated speed of the device. When the buffer is ready to receive/transmit another word from/to the computer, it can cause a program interrupt. Each device has an interrupt capability, and individual interrupt sources can be selectively enabled or disabled under program control to establish a flexible priority system.

The I/O bus can thus be time-shared between many devices all operating concurrently. Programmed I/O, and I/O under priority interrupt control, are standard features of the DDP-516. In addition, two high-speed modes of I/O are optionally available:

DMC - allows block transfers to/from memory via the I/O bus on an interlaced basis independent of program.

DMA - an alternate system whereby devices are interfaced to the DMA bus and data transfers are effected on a cycle stealing basis at rates of up to 1 million words per second.

Both of these options are described in Section IV.

Device Interface

A typical device interface contains the following functional units which are of concern to the programmer.

Data Buffer. -- One to 16 bits, accepts output data from computer and unloads to device, accepts input data from device and is unloaded to computer.

Address Decoder. -- Identifies the 6 bit device address.

Function Decoder. -- Identifies a 4 bit command from the computer.

Ready Flip-Flop. -- Is set when the data buffer is ready to accept/present data from/to the computer.

Interrupt Mask Flip-Flop. -- Can be set or reset by program. When set it allows the "ready" condition to cause an interrupt.

I/O Instructions

The INA, OTA, SKS and OCP instructions all include the device address in their six least significant (11-16) bit positions. Functions (commands or status tests) are contained in bits 7-10.

Input/output instructions are extremely powerful in that a single instruction:

a. Selects the device
b. Tests its ready status
   1. If Ready, transfers data and skips the next instruction.
   2. If Not Ready, proceeds to the next instruction.

Note that this organization possesses the following advantages for real-time processing:

a. Many devices can be operating concurrently, time-sharing the I/O bus on a multiplexed basis.
b. Selecting a device as part of an input/output instruction precludes the possibility of being interrupted between device select and data transfer.
c. The computer is never hung-up in a wait condition because of a device not being ready.

I/O Bus Lines

Table 3-1 lists the lines in the I/O bus. These include 16 data input lines (INB), 16 data output lines (OTB), 10 lines used for device address and function (ADB), ready line (DRL), priority interrupt lines (PIL), and various other timing and control lines.

INA Instruction. -- The INA instruction is used to input data from a device into the A-register via the input bus. All 16 bits of the data are ORed into the input bus by the instruction; however, data is not necessarily placed on all lines by every device. Thus, a character input device may place data only on the eight least significant bits of the input bus leaving the other bits as ZEROs. Since the content of the input bus may then be logically ORed with the A-register, the effect is as though only eight bits had been transferred from the device to the A-register. The function code portion of the INA instruction is typically used by the device to determine the mode of input (for example, binary or ASCII).

The INA instruction sends out its device and function code on the I/O bus. It then looks for a ready signal on the DRLIN (device ready line). If a ready signal is received within a predetermined time interval, the content of the INB (input bus) is logically ORed with the contents of the A-register and the next instruction is skipped. A reset-ready signal is also sent out on the RRLIN (reset ready line) to tell the device that the data has been

Table 3-1.
Input/Output Bus Lines

Lines Available for Input/Output	Designation	Bit Capacity	Function
Output bus	OTB_{1-16}	16	Transmit data from the computer to an I/O device
Input bus	INB_{1-16}	16	Transmit data from an I/O device to the computer
Address bus	ADB_{7-10}	4	Define the function to be performed by an I/O device
	ADB_{11-16}	6	Define the I/O device selected
Device ready line	DRLIN	1	Transmit a signal to the computer indicating the status of the device addressed by the I/O command
Output control pulse	OCPLS	1	Transmit a pulse from the computer that defines the fact that an OCP command is being executed
Master clear	MSTCL	1	Transmit a master reset to devices
Parity error	PARCK	1	Transmit a signal to the computer indicating that a parity error has been detected in an I/O device
Program-interrupt line	PIL00	1	Transmit a signal to the computer indicating that a standard interrupt is requested
Set Program interrupt mask	SMK01	1	Transmit a pulse from the computer indicating that the OTB contains a new setting for the interrupt mask flip-flops
Clear mask	CMKXX	1	Transmit a pulse from the computer used to clear the device mask control flip-flops
Set Mask (general)	SMKXX	1	Transmit a pulse from the computer indicating that the OTB contains a new setting for option masks specified by $ADB_{7-10;\ 14}$
Reset ready line	RRL1N	1	Transmit a pulse from the computer which is used to strobe the output bus during an OTA instruction and to "reset ready" during the OTA and INA instructions.

accepted by the computer. If bit 7 is set in the instruction, the A-register is cleared before the INB is ORed with the A-register. If a ready signal is not received, no input is performed and the next instruction is not skipped.

OTA Instruction. -- The OTA instruction is utilized to send data from the A-register to an output device. All 16 bits of the A-register are sent out on the I/O bus; however, not all may be accepted by a particular device. Thus, a character device might receive only the eight least significant bits of the data. The function code portion of the instruction is typically used by the device to determine the mode of output (for example, binary or ASCII).

This instruction sends out its device and function code and the contents of the A-register on the I/O bus. It then looks for a ready signal on the DRLIN (device ready line). If a ready signal is received within a predetermined time interval, an output pulse is sent out on the RRLIN line indicating to the device that it may take data off the OTB (output bus). The next instruction is then skipped. If a ready signal is not received, no output function is performed, and the next instruction is not skipped.

OCP Instruction. -- The OCP instruction is used to set up the operating mode of a device, to start the device, etc. This instruction sends out its device and function code on the I/O bus. It also sends an output control pulse on the OCPLS line after the device has had time to receive and decode the address and function bits. The function bits in this instruction are used to determine the particular function that the OCPLS pulse is required to perform. The DRLIN line is not examined during this instruction, and the next instruction is never skipped.

SKS Instruction. -- The SKS instruction is used to test different conditions in the device. Thus, it might test for "power on," "tape moving," "device busy," "device ready," etc. It is also used to supplement the device-ready test included in the INA and OTA instructions. The function bits are used to determine the particular condition to be tested.

This instruction sends out its device and function code on the I/O bus. It then looks for a status signal on DRLIN. If an affirmative status signal is received within the prescribed time interval, the next instruction is skipped. If an affirmative status signal is not received, the next instruction is not skipped.

Example: The following is an example of utilizing the programmed mode to input a block of data into memory.

```
        LDX - N          Load index with block length
        SKS '01XX        Device busy?
        JMP BUSY         Yes, Jum out
        OCP '00XX        No, start device
LOOP    INA '10XX        Input word to A and skip if ready
        JMP *-1          Loop if not ready
        STA AREA+N, 1    Store A register in memory
        IRS 0            Increment index register
```

```
JMP LOOP        If not end of block
OCP '01XX       Turn off device
```

Note that XX in the SKS, OCP and INA commands specify device address. Actual codes are listed in Appendix E.

Timing

The basic loop between successive input instructions consists of

INA	2 cycles
STA	2 cycles
IRS	3 cycles
JMP	1 cycle
Total:	8 cycles = 7.68 μsec

This determines the maximum frequency of I/O to/from memory in the programmed mode, which is 130,000 words per second. For higher data rates, a DMC or DMA must be used (see options).

Interrupt Mode

The DDP-516 has an interrupt system to which all devices are connected via the priority interrupt line (PIL) of the I/O bus. For a device to cause an interrupt, the following conditions must be met:

a. The device must be ready
b. The interrupt mask flip-flop must be set (see SMK instruction below)
c. System interrupt must be enabled by an ENB instruction.

All interrupts are stored until they are serviced. An interrupt request is removed by the action of an INA or OTA command resetting the ready status.

I/O interrupts are serviced at the end of an instruction unless they are delayed by higher priority systems such as DMC (see Section I, Memory Access Priority Structure). The action of the standard interrupt is to cause a forced indirect jump-store through location 63_8 (JST *63). This takes three cycles and also forces an Inhibit Interrupt (INH) instruction.

The interrupt subroutine (whose starting address is stored in 63_8) can then reset the mask flip-flop for lower-priority devices, leaving those of higher priority still set, and ren-enable interrupt. Upon exiting the interrupt subroutine it can then reset the lower priority mask again.

This allows the 516 to have a very flexible priority interrupt system, with high priority interrupts interrupting lower priority interrupts. Sixteen levels of interrupt can be controlled in one instruction by means of the SMK command.

SMK'20 Set Interrupt Mask Instruction. -- This is a modified OTA with a device address of 20_8. SMK'20 transfers the contents of the A register via the OTB to the mask flip-flops of various devices. Each bit position of the A register controls a unique device (see Table 3-2). A ONE sets the mask, a ZERO resets it. No ready test or skip is performed by this instruction. Since many interrupt sources can be activated simultaneously, the interrupt servicing subroutines will have to determine the source of the interrupt. This is implemented by executing SKS instructions for each device whose mask is set. These SKS's may also form a priority chain by testing the highest priority devices first.

The signals in the I/O bus which are used for interrupt are as follows.

a. PIL00 - This ORs together interrupt request signals from all standard interrupt sources and sends them to the CPU.

b. DRLIN - This line is used by the SKS instruction to test each individual interrupt source in order to check whether it is requesting an interrupt. The device address is sent out which selects the device, and a particular function code is sent out which places the status of the priority interrupt request logic on DRLIN.

c. SMK01 - This line from the CPU is used in place of a device address and a function code to indicate that a new status for the interrupt mask bits in the system is on the OTB.

Table 3-2.
Standard Interrupt Mask Assignments

OTB Bit No.	Device	OTB Bit No.	Device
1	Mag Tape Control Unit No. 1	9	Paper Tape Reader
2	Mag Tape Control Unit No. 2	10	Paper Tape Punch
3	(Unassigned)	11	ASR-33/35
4	Moving Head Disc File	12	Card Reader
5	I/O Channel No. 1	13	(Unassigned)
6	I/O Channel No. 2	14	Line Printer
7	I/O Channel No. 3	15	Memory Parity
8	Fixed Head Disc File	16	Real Time Clock

Power Failure Interrupt (PFI)

The basic computer contains a PFI circuit which acts as a memory protection feature. If the primary computer ac input power fails or is turned off at the control console while the computer is in the "RUN" mode, the PFI circuit either halts the computer or forces an interrupt to a pre-assigned memory location. The operation performed by the PFI on the detection of a power failure is dependent on the position of the console PFI/PFH control switch.

If the control switch is in the PFI position, the detection of a power failure will cause the PFI to initiate an interrupt during which the computer is forced to perform an indirect JST through memory location $(00060)_8$. The PFI interrupt will occur at least one millisecond before the dc power drops below the guaranteed operating limits of the circuits.

If the control switch is in the PFH position, the detection of a power failure causes the PFI to place the computer in a halt state. No information in memory will be altered when power fails.

Start Button Interrupt

A START button interrupt, which enables the computer operator to initiate an interrupt during the execution of a program by depressing the START button is also a standard feature. This will, in turn, result in execution of an indirect Jump and Store (JST) instruction through location 63_8 to any special-purpose routine the user may desire. This instruction has no mask control nor can it be tested with an SKS. To allow this interrupt the permit interrupt indicator must be set (ENB) and the computer must be executing instructions (not halted).

NOTE

On systems with extended addressing this interrupt and PFI will put the CPU in extended mode (EXTMD) see Section IV for details of this mode.

Program Interrupts

The program interrupt group includes (1) SI - Standard Interrupt, (2) PFI - Power Failure Interrupt, (3) PI - Priority Interrupt, and (4) ML - Memory Lockout Violation Interrupt. Interrupts of this type can occur only when the CPU has completed an instruction; the interrupt is accomplished by forcing the CPU to generate an indirect JST instruction to a dedicated location.

NOTE

A standard interrupt or a priority interrupt may only occur when the CPU is in the "permit interrupt" status; Memory Lockout Violation Interrupt and Power Failure Interrupt may occur regardless of the CPU "permit interrupt" status.

Computer Breaks

The computer break group includes (1) RTC - Real Time Clock Break, (2) MI - Memory Increment Break, (3) DMC - Direct Multiplex Control Break, and (4) DMA - Direct Memory Access Break. Real Time Clock, Memory Increment and DMC breaks can occur only when the CPU has completed an instruction. DMA breaks, however, may occur without waiting for the end of an instruction. All breaks may occur independent of the "permit interrupt" status.

SECTION IV
MAIN FRAME OPTIONS

EXTENDED ADDRESSING CONTROL FOR 24K AND 32K MEMORIES, MODEL 516-05-06

Memory expansion above 16K in the DDP-516 is handled by the introduction of the "extend" mode. The program counter bit (P02) provides the fifteenth bit of the 32K address field and conditions bit 2 of the Y-register (Y02) when the sector being addressed is not zero.

The extend mode changes the interpretation of the index bit of the indirect address word, which becomes part of a 15-bit indirect address. Only one level of indexing is possible in the extend mode. It is specified by bit 2 of the instruction word and is always the final operation in generating the effective operand address. (See Figures 4-1A, 4-1B, and 4-1C for flowgrams illustrating the operation of a system with extended addressing.

Operation

The Extended Mode Indicator (EXTMD) is set or reset by the generic instructions EXA or DXA, respectively, and by an OTK , set if $(A)_3$ is a ONE, reset if a ZERO. It is also set by the occurrence of a program interrupt. An indication that the computer is in an extend mode may be displayed at the control panel (refer to operating instructions given in Section VI.). A Previous Mode Indicator (PMI) is added to the mainframe to save the mode in which the program was operating when a program interrupt occurred.

The PMI is set if the CPU is in the extend mode when a priority interrupt occurs. It is reset if the CPU is not in the extend mode when a priority interrupt occurs and when the control panel MASTER CLEAR pushbutton is depressed.

Instruction Complement

Table 4-1 contains a list of instructions required for extended addressing.

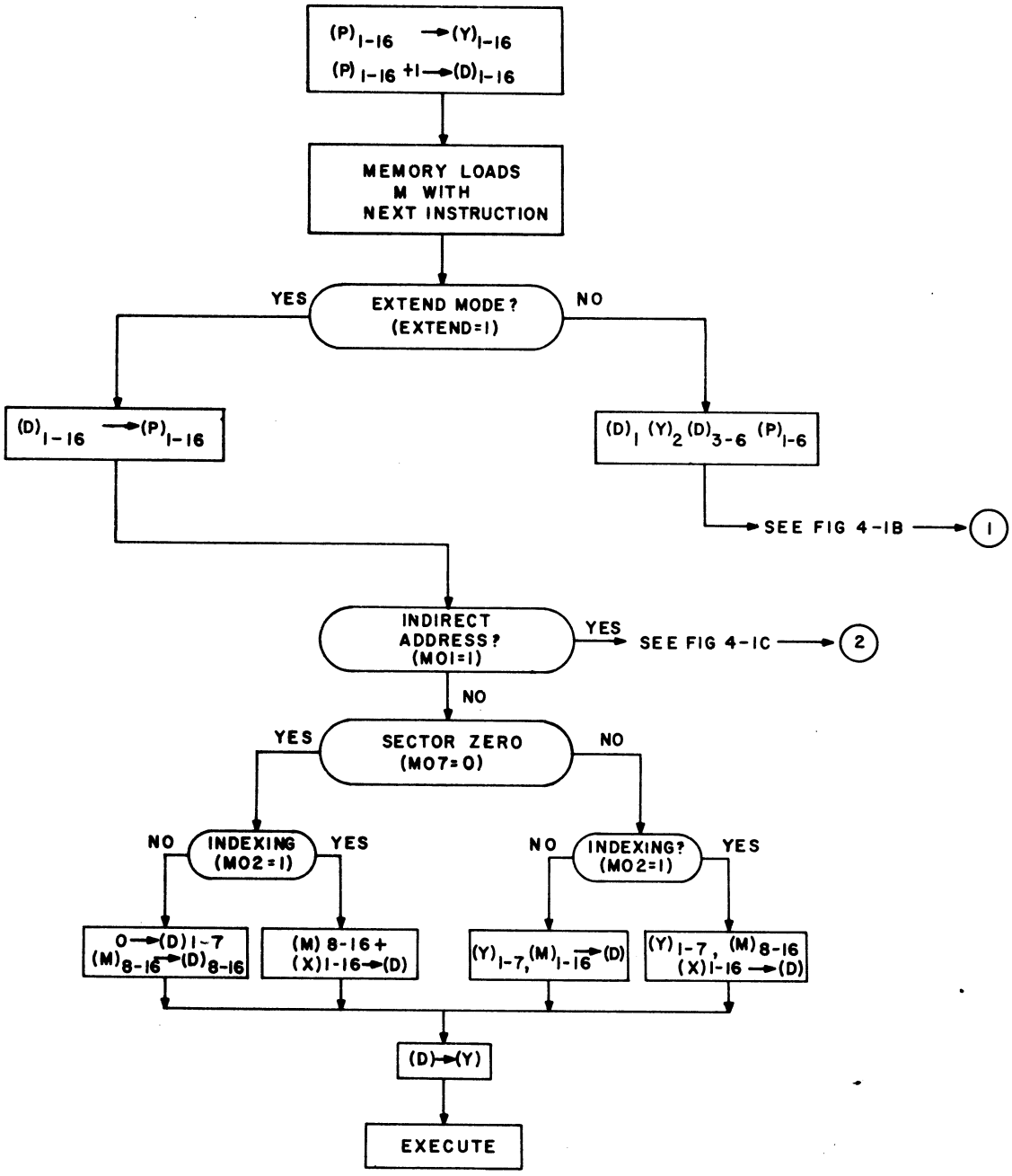


Figure 4-1A. Operation of a System with Extended Addressing, Flow Diagram (Sheet 1 of 3)

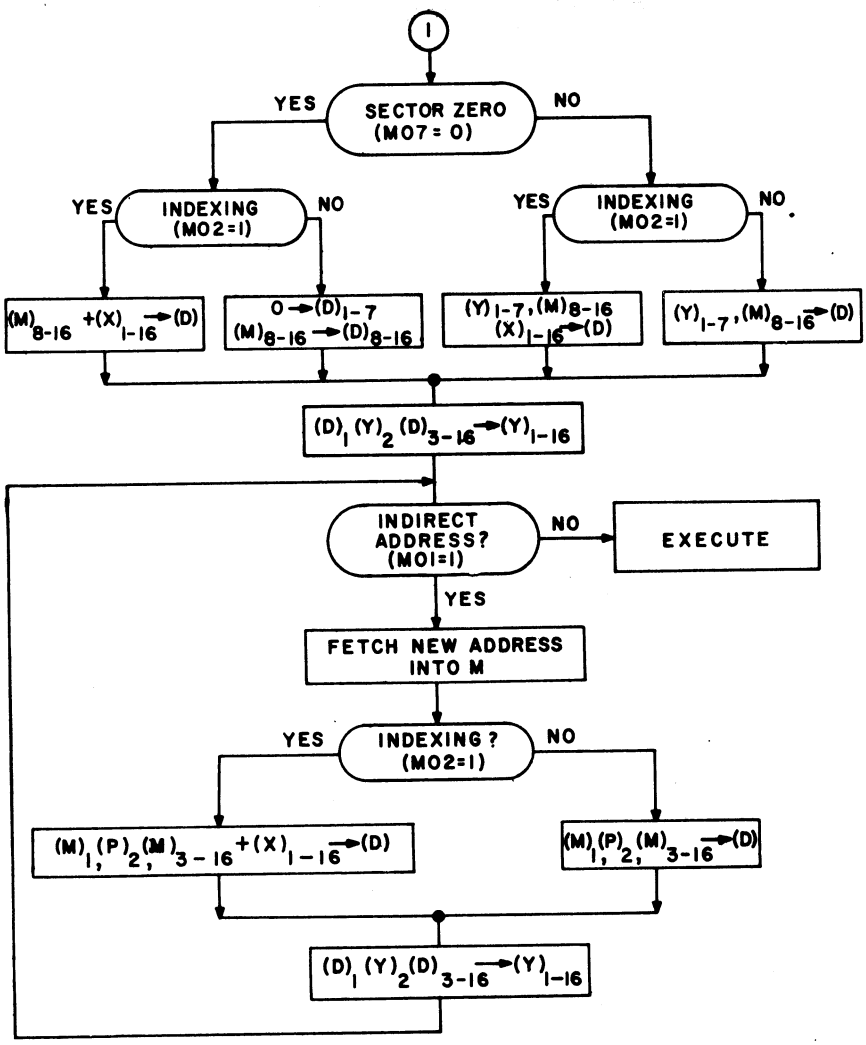


Figure 4-1B. Operation of a System with Extended Addressing, Flow Diagram (Sheet 2 of 3)

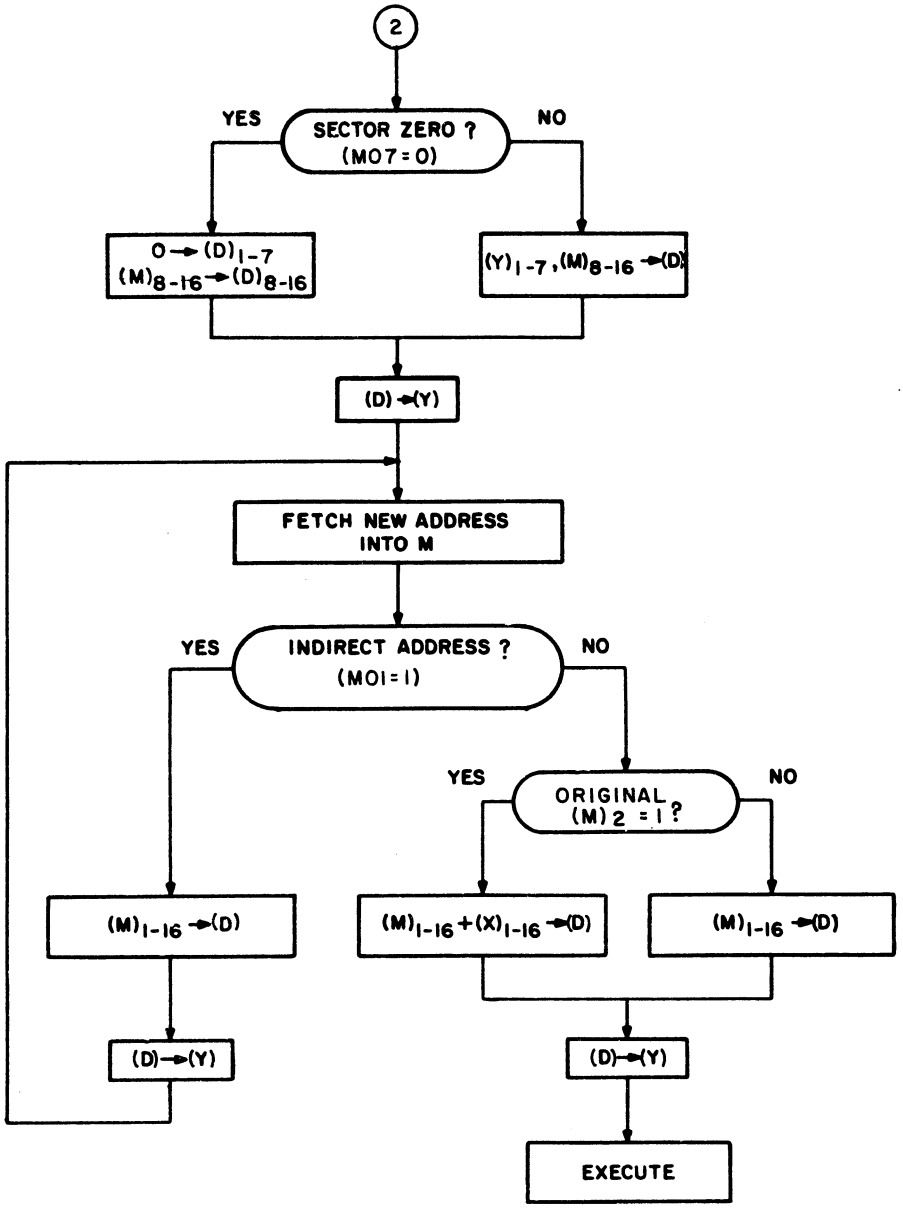


Figure 4-1C. Operation of a System with a 32K Memory, Flow Diagrams (Sheet 3 of 3)

Table 4-1
Extended Addressing Instructions

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
EXA*	G	000013	Enable Extended Addressing	Places computer in extend mode by setting EXTMD (Extend Mode Indicator)	1	0.96
DXA*	G	000011	Disable Extended Addressing	Restores computer to normal mode. Mode change not effective until after a JMP (01) has been executed to enable proper return from an interrupt subroutine. Any number of non-JMP instructions may be included between the DXA and the first JMP instruction.	1	0.96

*See INK, OTA instructions Table 2-2. EXTMD will reset on JMP (01) after disabling OTK. Same as DXA

NOTE

The extend mode alters the JST instruction to allow it to store a 15-bit program counter. Bit 1 of the memory location specified by the effective operand address is left unchanged.

MEMORY PARITY OPTION, MODEL 516-07

The memory parity option enables generation of parity on all memory write cycles and checking of parity on all memory read cycles. An exception exists in that parity is not checked during a console memory read operation. The memory parity error flip-flop in the computer is set when a memory parity error occurs and can be tested and reset under program control. It can also be displayed on the computer control panel (refer to Section VII). The MASTER CLEAR pushbutton switch on the control panel resets the parity error flip-flop. When the parity error flip-flop is set, an interrupt is generated on the standard interrupt line. This interrupt can be masked on or off by the parity error mask bit (bit 15).

Instruction Complement

The instructions added when this option is included in a system are listed in Table 4-2.

Table 4-2
Memory Parity Instructions

Mnemonic	Type	Instruction Word	Definition	Description	No. of Cycles	Time (μsec)
RMP	G	000021	Reset Memory Parity Error	Resets memory parity error flip-flop	1	0.96
SPS	G	101200	Skip on Memory Parity Error	Skips next instruction if parity error flip-flop is set	1	0.96
SPN	G	100200	Skip on No Memory Parity Error	Skips next instruction if parity error flip-flop is reset	1	0.96
SMK '0020	I/O	170020	Set Mask	$(A)_{15}$ → Parity Interrupt Mask 1. (A_{15}) = 1, enable interrupt 2. (A_{15}) = 0, inhibit interrupt	2	1.92

MEMORY LOCKOUT OPTION, MODEL 516-08

The memory lockout option facilitates the time-shared execution of various programs. The option provides base sector relocation to facilitate desectorization of more than one program. It also equips the CPU with a mode of operation called the "restricted mode" which enables unverified programs to be time-shared with other programs.

Base Sector Relocation

The memory lockout option provides for the relocation of the base sector insofar as the latter term applies to address information. The option includes a 6-bit base sector relocation register (J, non-readable) used to identify the physical sector currently assigned as the base sector. When the sector bit, bit 7 of the instruction word, is a one, the address (bits 8-16) is in the same sector as the instruction being performed. This represents no change from the basic machine. When the sector bit is a zero, the memory lockout option forces the address to be in the sector specified by the base sector relocation register. Figure 4-2 contains a flow chart that shows when base sector relocation takes place relative to indexing extended addressing and indirect addressing. Note if physical sector zero is called for as a result of indexing, it will not be relocated.

Base sector relocation does not affect memory references caused by breaks or program interrupts. The base sector relocation register can be changed by an SMK '1320 instruction (see Table 4-3). Any program interrupt, as well as MASTER CLEAR, clears this register.

Index register $(00000)_8$ and the hardware index register will not agree after the relocation of the base sector. Before any indexing is attempted, the relocated $(00000)_8$ should be modified (STA or LDX) to get the hardware register in step with the relocated $(00000)_8$. This operation must be repeated when the base sector is returned to sector zero.

Restricted Mode

There are two modes of operation associated with the memory lockout option; they are restricted and normal modes. The restricted mode has the following properties:

a. Instructions which normally write into memory locations can be "locked out" of protected memory sectors. These instructions are: STA, LDX, STX, IMA, IRS and JST.

b. Certain instructions are considered illegal and cannot be performed. They are: OCP, SKS, OTA, INA, SMK, HLT, and INH.

c. Indirect addressing is limited to eight levels.

If executed in the restricted mode, SMK, OTA, INA, OCP, and SKS instructions will cause a memory lockout violation and request an interrupt (location 00062_8) which will occur at the end of the violating instruction. OCP and SMK are treated as NOPs, SKS is unchanged, and an OTA or INA is treated as a SKS. If the device was ready (skip condition), the INA will set the A reg to all ones. For the SMK, OCP and the non-skip, (device not ready) case of OTA, INA, SKS, the interrupt JST will store the address of the violating instruction +1. For the skip cases of OTA, INA, SKS, the interrupt JST will store the address of the violating instruction +2.

If attempting to alter a location in a protected sector, while in the restricted mode, STA, STX, LDX, IMA, IRS, or JST will cause a memory lockout violation. The violating STA, STX or LDX will be treated as a NOP, IMA as a LDA, IRS as an IRS except that the protected memory location will not be modified, and the JST as an unconditional JMP to EA + 1. The memory lockout violation interrupt is strobed into the interrupt priority net-

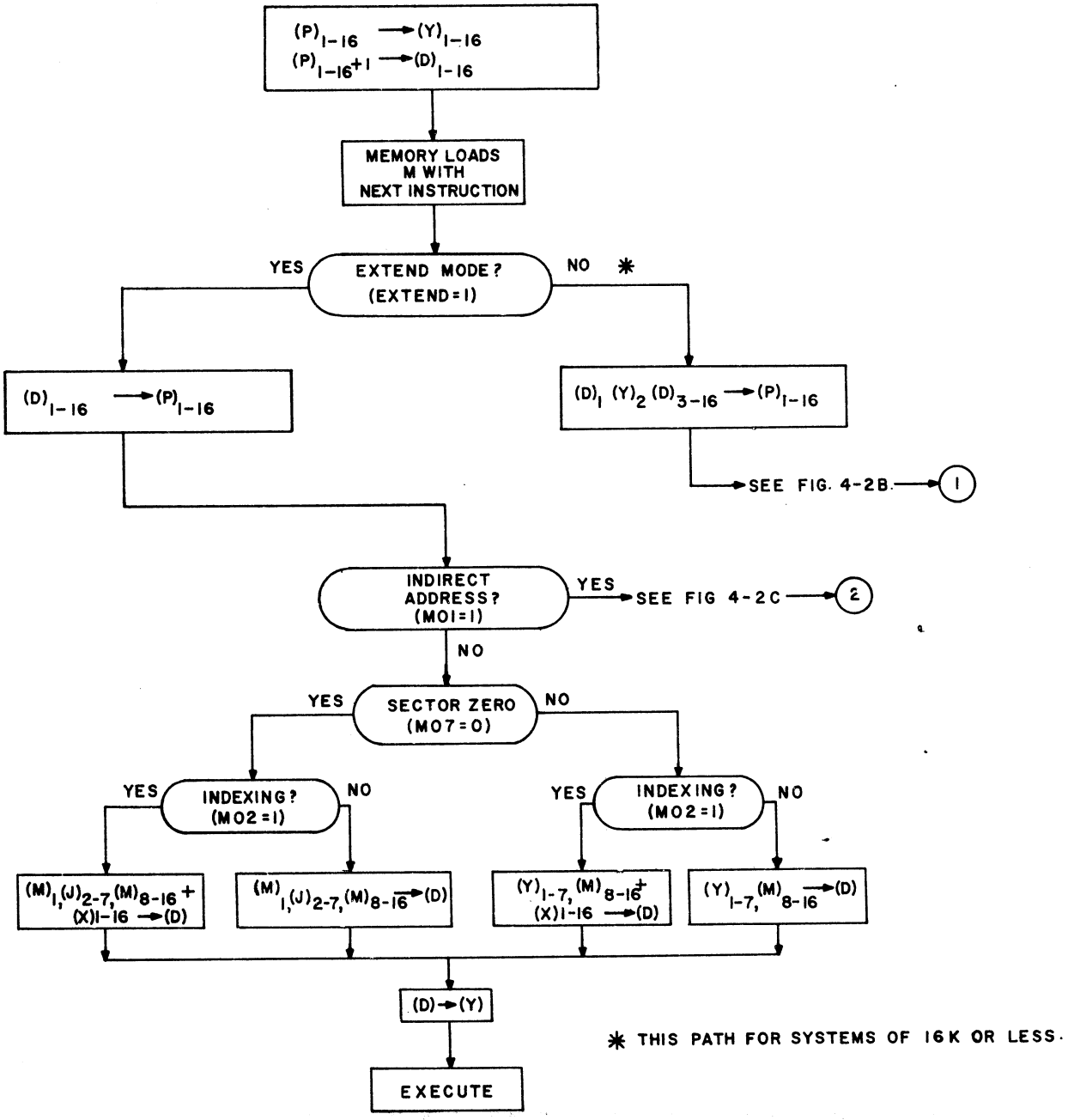


Figure 4-2A. Operation of a System with Memory Lockout and up to 32K of Memory

work during the next clock cycle after the completion of the violating instruction. There are three cases for this interrupt:

a. If the next clock cycle is a DMA, DMC, RTC, or MI cycle, the memory lockout violation interrupt will occur after such a cycle and the interrupt JST will store the address of the violating instruction +1.

b. If the next clock cycle is the next instruction in the program, it will be processed normally (subject to restricted mode operation) and the memory lockout violation interrupt will occur at the completion of this instruction. The interrupt JST will store the address of the violating instruction.

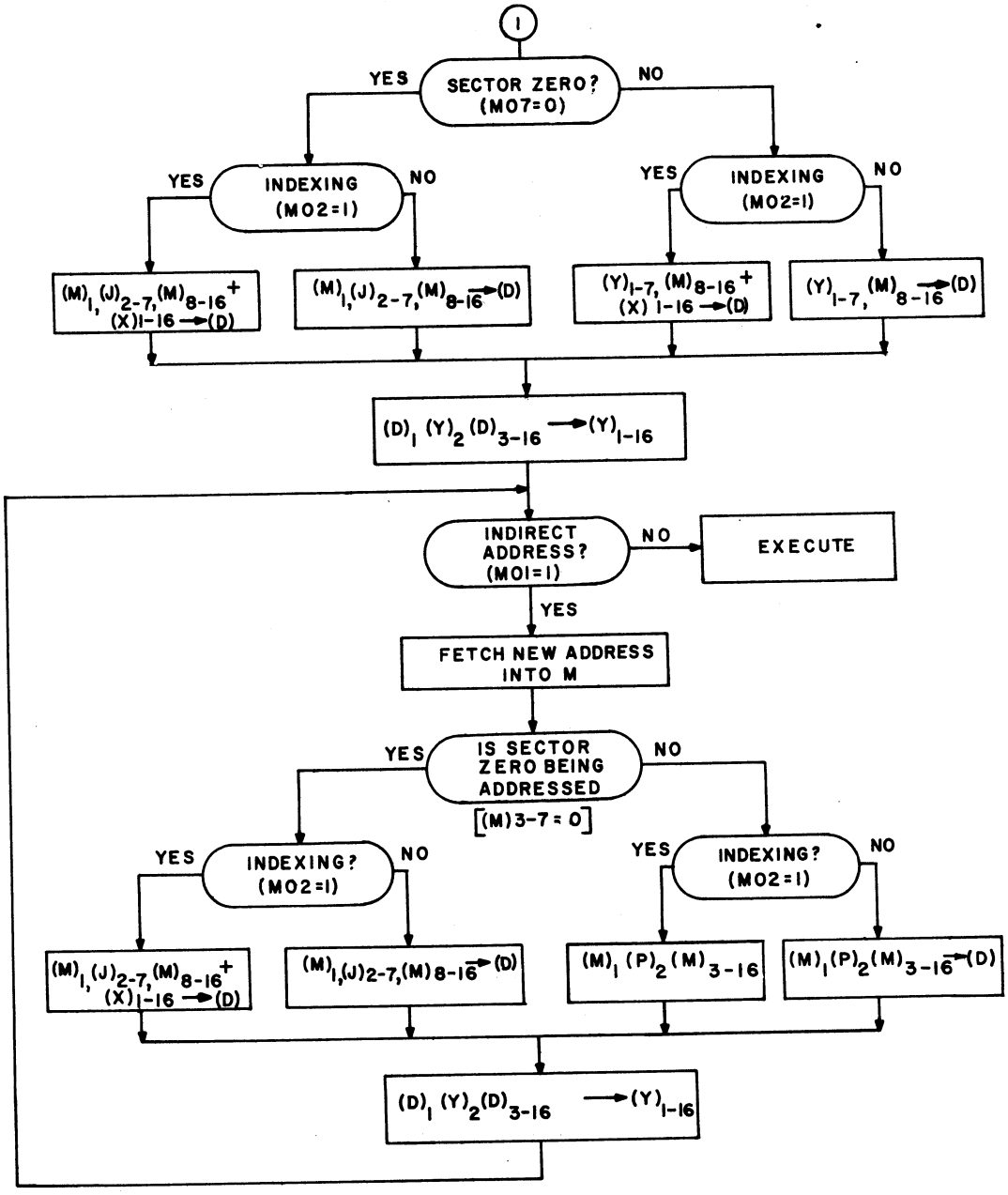


Figure 4-2B. Operation of a System with Memory Lockout and up to 32K of Memory

c. If a standard or priority interrupt was pending during the violating instruction, it will be processed at the end of the violating instruction and no memory lockout violation interrupt will be processed.

An HLT instruction will generate a memory lockout violation and will be treated as a NOP. The memory lockout violation interrupt will be processed in the same manner as STA, STX, etc.

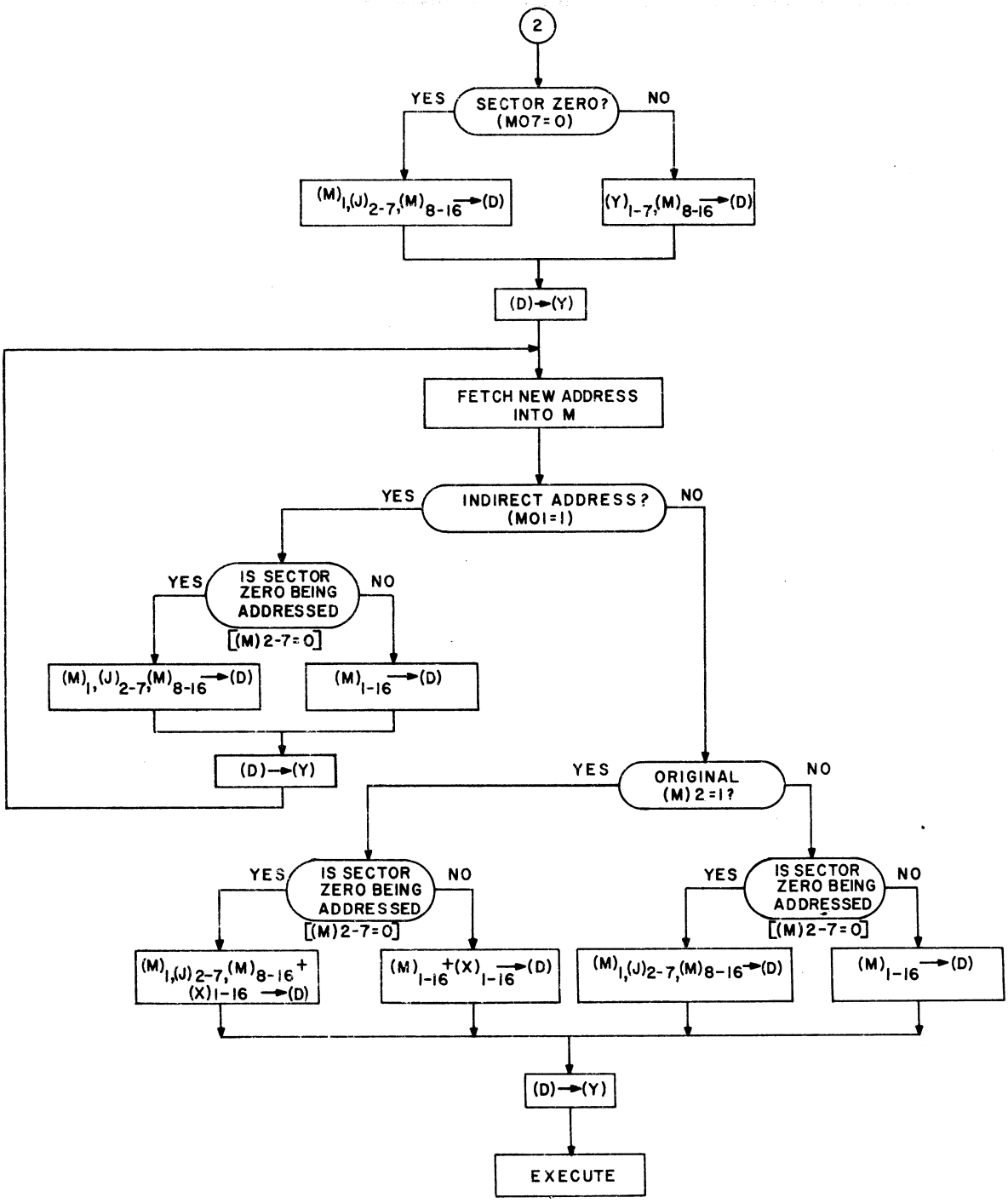


Figure 4-2C. Operation of a System with Memory Lockout and up to 32K of Memory

An INH instruction causes a memory lockout violation but does inhibit any standard or priority interrupt pending during its execution. The processing of the memory lockout violation interrupt is the same as STA, STX, etc, except case "c" does not apply.

Table 4-3
Memory Lockout Instructions

Mnemonic	Type	Instruction Word	Definition	Description	No of Cycles	Time (μsec)
ERM	G	001401	Enter Restricted Mode	Enables program interrupt and puts computer in restricted mode operation. Restricted operation continues until any program interrupt occurs. Does not take effect until after the next instruction is completed.	1	0.96
SMK '1320	I/O	171320	Set Relocation Register	$(A)_{2-7} \rightarrow (J)_{2-7}$ Defines physical location of all address references to base sector until another SMK '1320 is executed or MASTER CLEAR is activated, or any interrupt occurs.	2	1.92
SMK '1420	I/O	171420	Set Lockout Mask 1	$(A)1\text{-}16 \rightarrow (LMR)_{1-16}$	2	1.92
SMK '1520	I/O	171520	Set Lockout Mask 2	$(A)1\text{-}16 \rightarrow (LMR)_{17-32}$	2	1.92
SMK '1620	I/O	171620	Set Lockout Mask 3	$(A)1\text{-}16 \rightarrow (LMR)_{33-48}$	2	1.92
SMK '1720	I/O	171720	Set Lockout Mask 4	$(A)1\text{-}16 \rightarrow (LMR)_{49-64}$	2	1.92

The program interrupt to location $(00062)_8$, generated by an aborted instruction, cannot be masked off.

The restricted mode is entered by executing an ERM instruction. Visual indication of restricted mode operation is given through the use of the ML (memory lockout) indication on the console. Operation in the restricted mode is continuous until any program interrupt occurs. The MASTER CLEAR pushbutton places the machine in the normal mode.

The DMA, DMC, Real Time Clock and Memory Increment options are unaffected by the restricted mode since they are treated as agents of normal mode programs. This means that they can write in any memory location, even when they are sharing time with a program executed in the restricted mode.

Normal Mode

Normal mode operation is free of any restrictions and a program can execute any instruction in its repertoire.

Protected Sector Selection

Selection of those memory sectors which are to be protected is controlled by a lockout mask register (LMR). It is a 16-bit register (expandable to 64 bits) in which each bit is associated with one 512-word memory sector. A bit is zero if the corresponding sector is protected. The register is changed by an SMK instruction and cleared with the MASTER CLEAR pushbutton switch. Table 4-4 shows the specific memory ranges protected by SMK '1420, SMK '1520, SMK '1620, and SMK '1720.

Table 4-4
Protected Memory Ranges

A-Register Bit	SMK '1420	SMK '1520	SMK '1620	SMK '1720
1	00000-00777	20000-20777	40000-40777	60000-60777
2	01000-01777	21000-21777	41000-41777	61000-61777
3	02000-02777	22000-22777	42000-42777	62000-62777
4	03000-03777	23000-23777	43000-43777	63000-63777
5	04000-04777	24000-24777	44000-44777	64000-64777
6	05000-05777	25000-25777	45000-45777	65000-65777
7	06000-06777	26000-26777	46000-46777	66000-66777
8	07000-07777	27000-27777	47000-47777	67000-67777
9	10000-10777	30000-30777	50000-50777	70000-70777
10	11000-11777	31000-31777	51000-51777	71000-71777
11	12000-12777	32000-32777	52000-52777	72000-72777
12	13000-13777	33000-33777	53000-53777	73000-73777
13	14000-14777	34000-34777	54000-54777	74000-74777
14	15000-15777	35000-35777	55000-55777	75000-75777
15	16000-16777	36000-36777	56000-56777	76000-76777
16	17000-17777	37000-37777	57000-57777	77000-77777

NOTE

Locations 00001-00017 are always protected against all programs, restricted or normal. However, no $\overline{\text{MLO}}$ violation interrupt occurs if an attempt is made to write in these locations unless sector zero is protected and the machine is in the restricted mode.

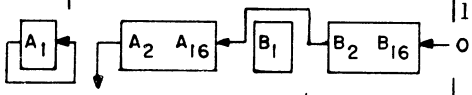
HIGH-SPEED ARITHMETIC UNIT OPTION, MODEL 516-11

This option enhances the arithmetic capability of the computer by providing hardware implementation of multiply, divide and normalize functions. The option also provides double-word load, store, add and subtract functions (double-precision mode). All multiply, divide and normalize functions are performed, automatically, in a double-precision mode; a special double-precision instruction must precede the performance of standard arithmetic operations if they are to be carried out in a double-precision mode (refer to Section I, Figure 1-3, for a description of double-precision machine words.)

Six optional instructions are added to the machine complement.whenever the high-speed arithmetic option is included in a system, and four instructions (LDA, STA, ADD, and SUB) have their execution modified. The optional instructions are listed and described in Table 4-5.

Instructions which reference double-precision operands must produce even effective addresses (after all indirection and indexing). An odd effective address will cause the instruction to be executed as if it had the next lower even effective address in the case of double load, add, or subtract. An odd effective address in a double-precision store will cause the B-register content to be stored in the specified location without affecting any other location.

Table 4-5.
High-Speed Arithmetic Unit Instructions

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μs)
MPY	MR	16	Multiply	(A) x [EA] → (A, B)	5.5	5.28
DIV	MR	17	Divide	(A, B) ÷ [EA] →(A) Remainder →(B) Overflow Status →(C) If initial magnitude of dividend is ≥ magnitude of divisor overflow occurs	10.0 or 10.5 or 11.0	9.60 or 10.08 or 10.56
NRM	G	000101	Normalize	 Shift until $(A)_2 \neq (A)_1$; number of shifts required stored as Shift Count	1 + n/2	0.96+ 0.48n
SCA	G	000041	Shift Count to A	Shift Count →$(A)_{11-16}$ 0 →$(A)_{1-10}$ The shift count is valid if no IAB, MPY, DIV, OTK, shift, or double-precision instruction has been executed since the last NRM instruction was executed.	1	0.96
DBL*	G	000007	Enter Double-Precision Mode	Execute LDA, STA, ADD, and SUB as DLD, DST, DAD and DSB, respectively, until SGL is executed or MASTER CLEAR is depressed	1	0.96
SGL*	G	000005	Enter Single-Precision Mode	Execute LDA, STA, ADD, and SUB in normal single precision	1	0.96
DLD	MR	02	Double-Precision Load	[EA] →(A) [EA+1] →(B)	3	2.88
DST	MR	04	Double-Precision Store	(A) →[EA] (B) →[EA + 1]	3	2.88
DAD	MR	06	Double-Precision Add	(A, B) + [EA, EA + 1] →(A, B) Overflow Status →(C) If $[EA + 1]_1 \neq (B)_1$, an invalid sum results		
DSB	MR	07	Double-Precision Subtract	(A, B)-[EA, EA +1] →(A, B) Overflow Status →(C) IF $[EA +1]_1 \neq (B)_1$, an invalid difference results	3 3	2.88 2.88

*See OTK, INK instructions Table 2-2.

REAL TIME CLOCK OPTION, MODEL 516-12

The Real Time Clock Option (RTC) permits the programmer to keep track of real time by automatically incrementing memory location $(00061)_8$. The frequency and stability of the incrementation is the same as the primary mainframe power source (50 or 60 cps ± 2 cps). With a 60 cps power source, the RTC will increment location $(00061)_8$ every 16.67 ms, with 50 cps source every 20 ms. Incrementing can be enabled or disabled with an OCP '0020 or OCP '0220 instruction, respectively.

When memory location $(00061)_8$ overflows from $(177777)_8$ to $(000000)_8$ the RTC causes a program interrupt via the standard interrupt line. The program interrupt can be inhibited or enabled with an SMK '0020 instruction (refer to Standard Interrupt Description in Section III). OTB 16 (A-register bit 16) is used to control the RTC interrupt. The interrupt can be tested by an SKS '0020 instruction and reset by an OCP '0220 or OCP '0020 instruction. If the RTC tries to interrupt when interrupt is masked off, it will wait until interrupt is enabled (by a proper SMK '0020 instruction) and then will cause an interrupt. Overflow from $(177777)_8$ to $(000000)_8$ does not inhibit incrementing.

Instruction Complement

The addition of the RTC option to a system adds three instructions to the basic system complement. The instruction which are added are described in Table 4-6.

Table 4-6.
Real Time Clock Option Instruction Complement

Mnemonic	Type	Instruction Word	Definition	Description	No. of Cycles	Time (μsec)
OCP '0220	IO	030220	Reset Program Interrupt Request and Stop Clock	This instruction inhibits the RTC and resets the program interrupt request. One more real time clock break may occur immediately following this instruction if the increment request occured during the execution of this instruction.	2	1.92
OCP '0020	IO	030020	Reset Program Interrupt Request and Run Clock	This instruction enables the RTC and resets the program interrupt request. The first increment request will occur within 0 to 16.7 ms following this instruction.	2	1.92
SKS '0020	IO	070020	Skip if RTC Not Interrupting	If the RTC is not requesting a program interrupt, the computer will skip the next instruction.	2	1.92

DIRECT MULTIPLEX CONTROL, MODEL 516-20

The Direct Multiplex Control (DMC) option permits data transfer between peripheral devices and the computer memory concurrently with computation.

When a device has data to input, or is ready to accept data, it uses the DMC control lines to request service. Devices request service from the DMC on lines called DIL. DIL line 1 has highest priority, line 16 has lowest. The priority network will allow the highest priority line which has its DIL set to be serviced by the next DMC cycle.

When a DMC cycle is required, the DMC will send a break request to the CPU. When the CPU has completed the current instruction, a DMC cycle will be executed. During this cycle the appropriate transfer between the device and the memory will take place, using the standard I/O bus.

This process is repeated each time the I/O device indicates that it is ready until the required number of words has been transferred. When the required number of words have been transferred, the DMC sends an End of Range (ERL) signal to the device. The device may use this signal to generate a program interrupt.

Up to 16 channels may be controlled by the DMC. Each channel requires a starting and ending address for the block transfer. These addresses (a pair per channel) are stored in dedicated memory locations (listed in Table 4-7).

Bit 1 of the starting address is used to specify input or output mode. A one in bit 1 sets the DMC in the input mode. A zero in bit 1 sets the DMC in the output mode. The remaining fifteen bits specify the starting address of the data block. In input mode, data from the device will be stored beginning at this address. In output mode, data beginning at this address will be sent to the device. The high order bit of the final address is not interpreted. The remaining 15 bits specify the address into or out of which the final transfer will take place.

Table 4-7.
DMC Start and Terminal Memory Address Locations

Channel Number	Starting Address	Ending Address
1	00020	00021
2	00022	00023
3	00024	00025
4	00026	00027
5	00030	00031
6	00032	00033
7	00034	00035
8	00036	00037
9	00040	00041
10	00042	00043
11	00044	00045
12	00046	00047
13	00050	00051
14	00052	00053
15	00054	00055
16	00056	00057

The DMC can effect a transfer following any instruction, provided a DMC request from a device is transmitted to the DMC 0.6 μsec before the end of that instruction. If a request occurs less than 0.6 μsec before the end of an instruction, the DMC cycle may not occur until after the next instruction.

The data transfer is completed 1.74 μsec into the DMC cycle for an input, 3.0 μsec for an output. Thus, the longest waiting time, from the time a request occurs to the time the data transfer is completed is:

$$T_{wc} = T_{li} + 3.84M + 1.2N + \begin{matrix} 2.34 & \text{(input)} \\ 3.60 & \text{(output)} \end{matrix}$$

where

T_{wc} = worst-case waiting time (μsec) from request to completion of data transfer.

T_{li} = execution time of longest* instruction (μsec).

*The longest useful instruction in the CPU repertoire is executed in 16.32 μsec. (Shifts of more than 32 places and memory reference instructions with more than six levels of indirect addressing are not considered "useful" in this context.) Lower values of T_{li} may be used to facilitate input-output buffer design, provided appropriate programming constraints are adopted.

M = number of higher priority DMC requests which may occur during T_{wc}.

N = number of DMA requests which may occur during T_{wc}.

Each DMC cycle requires four memory cycles, or 3.84 μsec, during which computation is suspended. At 0.6 μsec before the end of a DMC cycle the device request lines are inspected. If a device is requesting at this time, another DMC cycle will immediately follow the first. DMC cycles will continue as long as requests are waiting. During this time the CPU cannot resume control.

The maximum transfer rate of a single DMC channel is one word every four cycles or 260 KC. This rate can be attained if this channel is the only channel being used. If the DMC is operating at 260 KC, no computation can take place. In order to operate between 200 and 260 KC, T_{li} must be 0.96 μsec, for example an unconditional JMP*.

DMC Sub-Channel

A device is connected to the DMC control unit through a DMC sub-channel. The DMC sub-channel, available as an option on a number of standard I/O devices, contains the necessary logic to permit the device to operate in the DMC mode.

DMC Auto-Switch Option

The DMC Auto-Switch option provides automatic switching between two DMC sub-channels to permit the continuous transfer of data at high speed. To use the Auto-Switch option, one DMC sub-channel is set up as described above and the data transfer is started. While data is being transferred by the first DMC sub-channel, the second DMC sub-channel is set up. When the data transfer specified for the first sub-channel is complete, the Auto-Switch option automatically switches to the second DMC sub-channel and data transfer continues without interruption. An end-of-transmission interrupt occurs on the standard interrupt line to indicate that the switch has been made. The first DMC sub-channel must again be set up. When the data transfer specified for the second sub-channel is complete, the Auto-Switch option automatically switches back to the first sub-channel and interrupts. Switching is accomplished within one DMC cycle. This process is repeated continuously until the device is stopped or taken out of the DMC mode. Indicators associated with the device transferring data may be interrogated by the SKS instruction to determine which channel is active at any time and to determine which channel caused an interrupt.

DIRECT MEMORY ACCESS OPTION, MODEL 516-21

The direct memory access (DMA) option provides the central processor (CPU) with high speed input/output data transfer paths for addressing up to 32K of memory. The transfer rate is a mximum of one word every 0.96 μsec.

Applications

The DMA has the highest priority of all system options relative to memory access. The DMA is capable of interrupting between machine cycles such that any DMA interrupt request occurring during any cycle has access to memory at the end of that cycle. Note that the DMA is given access to memory without regard to whether or not the cycle just ended represents the completion of an instruction. These interrupts or breaks are for a minimum of 1200 ns for a single word transfer and 240 ns + N (960 ns) for continuous multi-word word transfers where N is the number of words transferred.

The DMA can effect a transfer following a memory cycle providing the request occurs 0.57 μsec before the end of cycle. However, requests arriving any later are serviced after the next memory cycle. The longest time between a request and the completion of the corresponding data transfer is 1.89 μsec for input transfers and 2.64 μsec for output transfers.

With few exceptions, all computation is momentarily suspended while a DMA cycle is in progress. The exceptions refer to the iterative instruction (e.g., LGL, LLL, LRR, etc.). These instructions comprise the shift/rotate group and the multiply/divide option. The execution of these instructions continues simultaneously with the DMA transfer cycle.

A DMA can have from one to four channels. The channels are arranged in a priority network with channel 1 having the highest priority and channel 4 having the lowest priority.

Each channel has a 16-bit address counter which stores the starting address and a 16 bit range counter which stores the two's complement of the block size. The most significant bit (bit 1) of the starting address is used to specify input or output mode. A ONE in bit 1 sets the DMA in the input mode. The remaining 15 bits specify the memory address from which the first transfer will occur. The range and address counters are incremented each time a data transfer occurs. Range counter overflow signifies the completion of a block transfer. This is accomplished by the generation of an end-of-range signal which is sent to each device and can be used to cause a program interrupt. The contents of the range counters can be read into the computer to determine whether an external stop signal has terminated the DMA operation before the specified number of words are transferred.

Instruction Complement

A listing of the instructions required for use with the DMA option is presented in Table 4-8.

The programming sequence for operating a device is:

1. Load Address Counter for Specific Channel (this will also clear the range register).
2. Load Range Register with two's complement of number of words to be transferred.
3. Activate Device.

DMA Auto-Switch

DMA Auto-Switch Option is available. It functions in a manner analogous to that previously described for the DMC Auto-Switch Option.

Table 4-8.
Direct Memory Access Instructions

Mnemonic	Type	Instruction Code	Definition	Description	No. of Cycles	Time (μsec)
SMK '0124	I/O	170124	Load Address Counter Channel 1	$(A)_{1-16} \rightarrow (AC1)_{1-16}$ $0 \rightarrow (RC1)_{1-16}$	2	1.92
SMK '0224	I/O	170224	Load Address Counter Channel 2	$(A)_{1-16} \rightarrow (AC2)_{1-16}$ $0 \rightarrow (RC2)_{1-16}$	2	1.92
SMK '0324	I/O	170324	Load Address Counter Channel 3	$(A)_{1-16} \rightarrow (AC3)_{1-16}$ $0 \rightarrow (RC3)_{1-16}$	2	1.92
SMK '0424	I/O	170424	Load Address Counter Channel 4	$(A)_{1-16} \rightarrow (AC4)_{1-16}$ $0 \rightarrow (RC4)_{1-16}$	2	1.92
SMK '1124	I/O	171124	Load Range Counter Channel 1	$(A)_{2-16} \vee (RC1)_{2-16}$ $\rightarrow (RC1)_{2-16}$	2	1.92
SMK '1224	I/O	171224	Load Range Counter Channel 2	$(A)_{2-16} \vee (RC2)_{2-16}$ $\rightarrow (RC2)_{2-16}$	2	1.92

Table 4-8. (Cont)
Direct Memory Access Instructions

Mnemonic	Type	Instruction Code	Definition	Description	Number of Cycles	Time (μsec)
SMK '1324	I/O	171324	Load Range Counter Channel 3	$(A)_{2-16}$ V $(RC3)_{2-16}$ → $(RC3)_{2-16}$	2	1.92
SMK '1424	I/O	171424	Load Range Counter Channel 4	$(A)_{2-16}$ V $(RC4)_{2-16}$ → $(RC4)_{2-16}$	2	1.92
INA '1124	I/O	13 1124	Read Range Counter Channel 1	If end-of-range, INA = NOP; otherwise, $1 \rightarrow (A)_1$ $(RC1)_{2-16} \rightarrow (A)_{2-16}$	2	1.92
INA '1224	I/O	13 1224	Read Range Counter Channel 2	If end-of-range, INA = NOP; otherwise, $1 \rightarrow (A)_1$ $(RC2)_{2-16} \rightarrow (A)_{2-16}$	2	1.92
INA '1324	I/O	13 1324	Read Range Counter Channel 3	If end-of-range, INA = NOP; otherwise, $1 \rightarrow (A)_1$ $(RC3)_{2-16} \rightarrow (A)_{2-16}$	2	1.92
INA '1424	I/O	13 1424	Read Range Counter Channel 4	If end-of-range, INA = NOP; otherwise, $1 \rightarrow (A)_1$ $(RC4)_{2-16} \rightarrow (A)_{2-16}$	2	1.92

PRIORITY INTERRUPT OPTION, MODEL 516-25/25-1

A multilevel priority interrupt system is available as an option. This option eliminates the need for an interrupt service routine to determine which one of the available interrupt lines caused an interrupt. A unique memory location is dedicated to each interrupt line. These locations are utilized in the same manner as the standard interrupt location is utilized in the standard interrupt system. When an interrupt occurs, the computer generates an indirect jump and store location instruction (JST) referencing the memory location dedicated to the source of the interrupt. Execution time of the computer-generated JST instruction is three cycles unless bit 1 of the dedicated location is a ONE. A ONE in this bit location indicates further indirect addressing; an additional cycle is required for each additional level of indirect addressing. Included in the option is a mask register which permits individual interrupt lines to be enabled and disabled under program control. This permits the relative priority of the interrupt lines to be established by the programmer.

The interrupt option is provided in groups of four interrupt lines. Up to 12 groups or a total of 48 interrupt lines can be handled by the system. The interrupt lines are consecutively numbered, and have decreasing priority with increasing number. The standard interrupt line is designated line 0 and retains its standard location $(63)_8$. The dedicated locations for the optional interrupt lines are shown in Table 4-9. On systems with more than 16K of memory, the occurrence of a program interrupt will cause the CPU to go into extend mode. See extended addressing for details of operation in this mode.

Priority Interrupt Control

Program interrupts requested by Priority Interrupt lines are individually controlled by mask bits associated with each group of interrupt lines. In addition, all Priority Interrupt lines are controlled by the INH and ENB instructions. Priority interrupt is inhibited until an ENB instruction has been executed. Following the execution of an ENB instruction, an interrupt will be accepted on any interrupt line having its associated mask bit set (one). Interrupt remains enabled until an INH instruction is executed or an interrupt occurs on any enabled line (forced INH). Following an interrupt or the execution of an INH instruction, interrupts will be inhibited until an ENB instruction is executed.

Table 4-9.
Dedicated Locations for the Twelve Groups
of Priority Interrupt Lines

Priority Interrupt Group	Dedicated Locations (Octal Codes)
1	00064 - 00067
2	00070 - 00073
3	00074 - 00077
4	00100 - 00103
5	00104 - 00107
6	00110 - 00113
7	00114 - 00117
8	00120 - 00123
9	00124 - 00127
10	00130 - 00133
11	00134 - 00137
12	00140 - 00143

The mask bits associated with each group of interrupt lines are controlled by SMK '0X20 instructions. These instructions set the appropriate bit in the mask register if the corresponding bit in the A-register is a ONE and reset the mask register bit if the corresponding A-register bit is a ZERO. Table 4-10 shows the mask assignments for the optional interrupt lines and the SMK instructions that service them.

NOTE

If an interrupt request occurs during the execution of an SMK instruction disabling that interrupt, the interrupt may or may not be accepted (depending on the exact timing of the interrupt signal with respect to the execution of the SMK instruction); therefore, the interrupt mask register should be changed only when interrupt is inhibited.

Table 4-10.
Priority Interrupt Mask Assignments

A-Register Bit No.	SMK '0120	SMK '0220	SMK '0320
1	1	17	33
2	2	18	34
3	3	19	35
4	4	20	36
5	5	21	37
6	6	22	38
7	7	23	39
8	8	24	40
9	9	25	41
10	10	26	42
11	11	27	43
12	12	28	44
13	13	29	45
14	14	30	46
15	15	31	47
16	16	32	48

Interrupt Line Number

MEMORY INCREMENT OPTION, MODEL 516-26

Groups of four priority interrupt lines may be optionally changed to memory increment break lines. Any number of priority interrupt groups may be so modified; however, the modified groups must be consecutive starting with the first group of four lines.

The function performed by a memory increment break is:

$$[\text{Ded. Location}] + 1 \rightarrow [\text{Ded. Location}]$$

There is no overflow indication and no interrupt generated on overflow. Execution of the break requires three cycles.

NOTE

Memory increment requests are not subject to control by the INH or ENB instructions; however, mask register bits are associated with memory increment lines for individual line control as described under Priority Interrupt Control, above. This interrupt does not cause the CPU to go into the extend mode.

SECTION V
INPUT/OUTPUT CHANNELS AND DEVICES

A DDP-516 system can include a variety of I/O devices in addition to the standard ASR-33/35. The optional devices, as well as the standard, can be used in a number of ways. They can be programmed by using FORTRAN IV, standard I/O library subroutines, or special-purpose user-prepared DAP programs. The FORTRAN IV Manual, Doc. No. 130071364, contains useful information regarding FORTRAN I/O statements and format specifications. Users who would like to operate I/O devices using standard I/O library subroutines will find complete documentation in the DDP-516 Users Guide (Doc. No. 130071627). Those who wish to prepare their own special-purpose I/O programs will find much helpful information in the following pages. Included in this section are discussions of:

ASR-33/35, Model 516-53/55, 516-56
High-Speed Paper Tape Reader, Model 516-50
High-Speed Paper Tape Punch, Model 516-52
Parallel I/O Channels, Model 516-32/33/34
SKS/OCP, Model 516-29
Card Reader, Model 516-61
Line Printer, Model 5-16-7050
Magnetic Tape System, Model 516-4100
Fixed Head Disc File, Model 516-4400
Moving Head Disc File, Model 516-4600
Process Interface Controller (PIC), Model 516-8100

ASR-33/35 TELETYPE UNITS, MODEL 516-53/55, 516-56

The ASR-33/35 Teletype Unit is the basic I/O device for the DDP-516 computer. The ASR-33/35 is a versatile device that prints out data from the computer or transmits data to the computer from the keyboard at the rate of ten characters per second. It can also read and punch paper tape at the same rate. In the local mode the unit may be used for off-line paper tape preparation, reproduction, or listing.

Keyboard and Carriage Features

The ASR-33/35 keyboard is similar to that of a standard typewriter. The keyboard contains four rows of keys that generate an eight-level internal code (see Figure 5-1 and Table 5-1). Letters and numerals are transmitted without a shift, similar to lower-case transmissions on a typewriter. Special characters (?, =, *, etc.) are typed by using the shift key, similar to upper-case positions on certain typewriters. Control functions, generated by using the control (CTRL) key, are X-OFF (S key), X-ON (Q key), EOM (C key), and BELL (G key). The LINE FEED and RETURN codes are transmitted without the CTRL key being depressed.

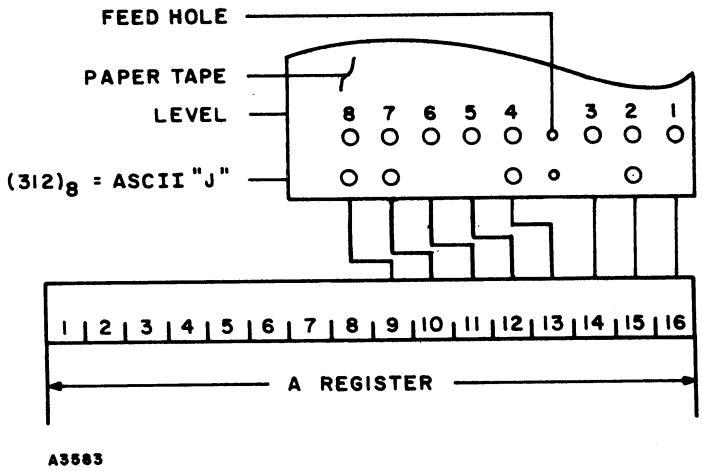


Figure 5-1. ASR-33/35 Paper Tape Format

The ASR-33/35 can print up to 71/75 characters per line. A carriage return and line feed must be executed after the last character to be printed in each line.

The ASR-33/35 keyboard is interlocked for all keys except the SHIFT, CTRL, and REPT keys, preventing more than one key being depressed at one time. The keyboard does not lock in the upper-case position so the operator must hold the SHIFT key depressed to produce special (upper-case) characters.

Table 5-1.
ASR-33/35 Character and Symbol Codes

Code	Page Printer	Code	Page Printer	Code	Page Printer	Code	Page Printer
000	Null *	040	Space	100	@	140	@
001	Null	041	!	101	A	141	A
002	Null	042	"	102	B	142	B
003	Null	043	#	103	C	143	C
004	Null	044	$	104	D	144	D
005	Null	045	%	105	E	145	E
006	Null	046	&	106	F	146	F
007	Bell	047	'	107	G	147	G
010	Null	050	(	110	H	150	H
011	Null	051	)	111	I	151	I
012	LF	052	*	112	J	152	J
013	Null	053	+	113	K	153	K
014	Null	054	,	114	L	154	L
015	Null	055	-	115	M	155	M
016	Null	056	.	116	N	156	N
017	Null	057	/	117	O	157	O
020	Null	060	0	120	P	160	P
021	Null	061	1	121	Q	161	Q
022	Null	062	2	122	R	162	R
023	Null	063	3	123	S	163	S
024	Null	064	4	124	T	164	T
025	Null	065	5	125	U	165	U
026	Null	066	6	126	V	166	V
027	Null	067	7	127	W	167	W
030	Null	070	8	130	X	170	X
031	Null	071	9	131	Y	171	Y
032	Null	072	:	132	Z	172	Z
033	Null	073	;	133	[	173	[
034	Null	074	<	134	\	174	Null
035	Null	075	=	135	]	175	Null
036	Null	076	>	136	↑	176	Null
037	Null	077	?	137	←	177	Null

* Whenever the Here Is Key is depressed (available on ASR-33 only) the answer back drum is activated, producing a burst of twenty characters of all zeroes.

Table 5-1. (Cont)
ASR-33/35 Character and Symbol Codes

Code	Page Printer	Key Depressed		
		Lower Case	Simult. Control	Simult. Shift and Control
200	Null			P
201	Null		A	
202	Null		B	
203	Null		C	
204	Null		D	
205	Null		E	
206	Null		F	
207	Bell		G	
210	Null		H	
211	Null		I	
212	LF	LF	J	
213	Null		K	
214	Null		L	
215	CR	CR	M	
216	Null		N	
217	Null		O	
220	Null		P	
221	X-ON		Q	
222	TAPE		R	
223	X-OFF		S	
224	Null		T	
225	Null		U	
226	Null		V	
227	Null		W	
230	Null		X	
231	Null		Y	
232	Null		Z	
233	Null			K
234	Null			L
235	Null			M
236	Null			N
237	Null			O

Table 5-1. (Cont)
ASR-33/35 Character and Symbol Codes

Code	Page Printer	Key Depressed			
		Lower Case	Simult. Shift	Simult. Control	Simult. Shift and Control
240	Space	Space Bar		Space Bar	
241	!		1		1
242	"		2		2
243	#		3		3
244	$		4		4
245	%		5		5
246	&		6		6
247	'		7		7
250	(		8		8
251	)		9		9
252	*		:		:
253	+		;		;
254	,	,		,	
255	-	-(minus)		-(minus)	
256	.	.		.	
257	/	/		/	
260	0	0		0	
261	1	1		1	
262	2	2		2	
263	3	3		3	
264	4	4		4	
265	5	5		5	
266	6	6		6	
267	7	7		7	
270	8	8		8	
271	9	9		9	
272	:	:		:	
273	;	;			
274	<		,		,
275	=		-	Alt Mode	-
276	>		.		.
277	?		/	Rub Out	?

Table 5-1. (Cont)
ASR-33/35 Character and Symbol Codes

Code	Page Printer	Key Depressed	
		Lower Case	Simult. Shift
300	@		P
301	A	A	
302	B	B	
303	C	C	
304	D	D	
305	E	E	
306	F	F	
307	G	G	
310	H	H	
311	I	I	
312	J	J	
313	K	K	
314	L	L	
315	M	M	
316	N	N	
317	O	O	
320	P	P	
321	Q	Q	
322	R	R	
323	S	S	
324	T	T	
325	U	U	
326	V	V	
327	W	W	
330	X	X	
331	Y	Y	
332	Z	Z	
333	[		K
334	\		L
335	]		M
336	↑		N
337	←		O

Table 5-1. (Cont)
ASR-33/35 Character and Symbol Codes

Code	Page Printer	Code	Page Printer	Lower Case
340	@	360	P	
341	A	361	Q	
342	B	362	R	
343	C	363	S	
344	D	364	T	
345	E	365	U	
346	F	366	V	
347	G	367	W	
350	H	370	X	
351	I	371	Y	
352	J	372	Z	
353	K	373	[	
354	L	374	Null	
355	M	375	Null	
356	N	376	Null	
357	O	377	Null	Rub Out

Notes:

1 Whenever the Break Key is depressed, a 000code will be generated as long as the key is held depressed. However, when the key is released, an indeterminate character will be produced.

2 The symbols appearing in the "Page Printer" column indicate the reaction of the printer to codes received on the line in output mode and to codes generated by the reader or keyboard in input mode. Null indicates no printing and no spacing.

3 No entry in the "Key Depressed" column indicates inability of the keyboard to produce that code.

4 The punch will perforate all codes transmitted in input or output mode. On the ASR-35 only, the first "Tape On" character and its associated rub out character, if character buffering is used for automatic punch control will not be punched.

ASR-33/35 On-Line Operating Modes

There are two basic modes of operation for the ASR-33/35 when on line: input mode and output mode. These are set up by the appropriate OCP instruction. Once set up, the ASR-33/35 remains in a given mode until it is changed by another OCP.

Input Mode. -- The input mode is used to transmit information from the ASR-33/35 keyboard to the computer or from the reader to the computer. In either case, printed copy is produced if the 8-bit character is printable, and a control function is performed if the 8-bit character is a control character (see Appendix B). If characters are being read from the reader, any of the 256 possible 8-bit characters appearing on the tape will be transmitted to the computer. When an X-OFF is read, the reader will stop after reading the character (two characters for ASR-35 except as described later) following the X-OFF, unless that following character is an X-ON. Master clear places the ASR-33/35 in the input mode.

Output Mode. -- The output mode is used to transmit information from the computer to the ASR-33/35 printer or the printer and the punch. In either case, printed copy is produced if the 8-bit character is printable, and a control function is performed if the 8-bit character is a control character. When punching, any 8-bit code transmitted from the computer will be punched whether it is printable or not. However, certain 8-bit codes -- $(221)_8$, $(021)_8$, $(005)_8$, and $(205)_8$ -- when transmitted from the computer will also cause a control action by the ASR-33/35 and prevent proper transmission of further characters. X-ON, $(221)_8$ or $(021)_8$ will start the paper tape reader, and WRU, $(205)_8$ or $(005)_8$ will trigger the answer-back drum.

Character Modes

Within either the input or output modes, either of two character modes, ASCII or binary, may be used. Code type is selected by individual INA or OTA instructions and may be intermixed in any manner (though this is not normally done).

ASCII Mode. -- In the ASCII mode a full 8-bit character is transmitted between the least significant 8 bits of the A-register and the ASR-33/35. This permits transmission of any standard character or control character from the reader or keyboard of the ASR-33/35 to the computer or from the computer to the printer or punch.

Binary Mode. -- In the binary mode a 6-bit character is transmitted to or from the least significant 6 bits of the A-register and the ASR-33/35. In the case of output in the binary mode, an additional 2 bits are automatically added in the high-order position to the 6-bit character to form a printable 8-bit character rather than a control character. On input, the two high-order bits of the 8-bit character transmitted by the ASR-33/35 are stripped and ignored.

ASR-33 Operation

Reader Control. -- The reader can be started under program control as follows:

a. Enable output mode with OCP '0104
b. Output an X-ON character (221_8) using OTA '0004
c. Delay until not busy (test with SKS '0104)
d. Enable in input mode with OCP '0004

Manual starting is controlled with the START/STOP switch. The first character to be read when the reader has been started is the one initially positioned over the read pins.

When operating under manual or program control, the reader stops upon recognition of an X-OFF character. The X-OFF and one following character will be transmitted to the device buffer before the reader stops. Manual stopping is controlled by the START/STOP switch. The reader will stop automatically if it runs out of paper tape. An X-OFF character will stop the reader when reading tape off-line. To continue reading, the operator can restart the reader by depressing the START switch.

Punch Control. -- The punch is controlled by manual operation of the punch ON/OFF switch. When the punch is on, any input from or output to the ASR-33 will cause tape to be punched. Tape leader can be generated in bursts of 20 sprockets with each depression of the HERE-IS key.

Off-Line Operation. -- Off-line operation of the ASR-33 includes the following.

a. Keyboard to printer
b. Keyboard to printer and punch
c. Reader to printer
d. Reader to printer and punch.

ASR-35 Operation

The ASR-35 operates in either on-line or off-line modes as described in the following paragraphs.

Off-Line. --

K Mode	Keyboard to printer
KT Mode	Keyboard to printer and punch Reader to printer and punch
T Mode	Keyboard to punch Reader to printer

On-Line. --

K Mode	Input transfer from keyboard monitored by printer (ASCII) Output transfer to printer (ASCII)
KT Mode	Input transfer from keyboard monitored by printer and punch if enabled (ASCII) Input transfer from reader monitored by printer and punch if enabled (ASCII or binary) Output transfer to printer and punch if enabled (ASCII or binary)
T Mode	Input transfer from reader monitored by printer (ASCII or binary) Output transfer to printer (ASCII) Simultaneous off-line operation of keyboard to punch (ASCII)
TTS Mode	Input transfer from reader (any eight-level code). Manual control of reader only. Automatic start and stop code inoperative. Simultaneous off-line operation of keyboard to punch (ASCII)
TTR Mode	Output transfer to punch (any eight-level code).

Reader Control (KT and T Modes Only). -- To start the reader under program control, the program must output an X-ON character (021_8 or 221_8). After waiting until the ASR is not busy, an OCP '0004 should be issued to enable the ASR in the input mode before proceeding with input transfer instructions. The reader can also be started by depressing the START switch and rotating the reader manual control switch to the ON position. When started, the first character to be read is the one positioned over the read pins.

When operating under program control, the reader will stop two characters after the recognition of an X-OFF character (023_8 or 223_8). The X-OFF character is read into the character buffer, and the next two characters are also read into the character buffer before the tape stops (unless the character following the X-OFF is RUBOUT, in which case only the RUBOUT is read). When operating under program control, the reader cannot be stopped manually, or by an X-OFF when operating off-line.

Punch Control (KT Mode, On-Line Only). -- To enable the punch when operating under program control, the program must output a TAPE character (022_8 or 222_8). A RUBOUT character or a time delay equal to one character time must follow the TAPE character. (The RUBOUT character will not be punched on paper tape.) Additional output transfers will then be punched on paper tape as required.

To stop the punch when operating under program control, the program must output an X-OFF character followed by a RUBOUT character. Both characters will be punched on tape.

Tape leader can be generated off-line on the ASR-35 by depressing the BREAK button until the required amount of leader is punched. The operator may then depress the BACKSPACE and RUBOUT keys to product a frame of all ONEs in place of the indeterminate frame produced when the BREAK button is released.

Programming

The control codes assigned to the ASR-33/35 are described in the following paragraphs. In summary they are as follows:

OCP '0004	Enable ASR-33/35 in input mode
OCP '0104	Enable ASR-33/35 in output mode
SKS '0004	Skip if ASR-33/35 is ready
SKS '0104	Skip is ASR-33/35 is not busy
SKS '0404	Skip if ASR-33/35 is not interrupting
SKS '0504	Skip is stop code was not read on ASR-33/35
INA '0004	Input in ASCII mode if ready
INA '0204	Input in binary mode if ready
INA '1004	Clear A and input in ASCII mode if ready
INA '1024	Clear A and input in binary mode if ready
OTA '0004	Output in ASCII mode if ready
OTA '0204	Output in binary mode if ready
SMK '0020	Set interrupt mask.

Enable ASR-33/35 in Input Mode (OCP '0004). -- This instruction sets up the device interface to accept characters from the ASR-33/35. It should be given any time it is desired to switch the ASR-33/35 from the output mode to the input mode. This instruction must not be given while the ASR-33/35 is busy. An SKS '0104 test should precede this instruction.

Enable ASR-33/35 in Output Mode (OCP '0104). -- This instruction sets up the device interface to transmit characters to the ASR-33/35. The instruction must be given any time it is desired to switch from the input to the output mode. The instruction must not be given while the ASR-33/35 is busy. An SKS '0104 test should precede this instruction.

Skip if ASR-33/35 Is Ready (SKS '0004). -- This instruction tests whether the ASR-33/35 device interface is ready to accept another character from the computer or to present another character to the computer.

Skip If ASR-33/35 Is Not Busy (SKS '0104). -- The ASR-33/35 busy signal is defined as follows:

a. In the output mode the ASR-33/35 is busy from the time a character is transmitted from the computer to the ASR-33/35 device interface until it has been serially shifted out to the ASR-33/35. This time is approximately 105 ms.

b. In the input mode the ASR-33/35 is busy from the time the ASR-33/35 starts to serially transfer a character to the device interface until the transfer is complete and the ASR-33/35 ready condition is present. This time is approximately 100 ms.

Skip If ASR-33/35 Is Not Interrupting (SKS '0404). -- This instruction tests whether the ASR-33/35 has caused an interrupt on the standard interrupt line.

Skip If Stop Code Was Not Read on ASR-33/35 (SKS '0504). -- This instruction tests whether a stop code (223_8 or 023_8) has been read by the ASR-33/35. The stop code indication can be tested as soon as the stop code has been read from the ASR-33/35 into the device buffer and is ready for input to the computer. When a stop code is read by an ASR-33/35, the stop code and one/two following characters will be transferred to the device buffer before the reader stops. The stop code indication will remain present until the character following the stop code is ready for input to the computer (approximately 100 ms).

Input in ASCII Mode If Ready (INA '0004). -- This instruction transmits the full 8-bit character from the ASR-33/35 to the 8 least significant bits of the A-register. The A-register is not cleared. Ready must be honored within 1 ms to ensure transmission. If Ready is true, the instruction will be executed and the next instruction skipped. If Ready is not true, this instruction will be treated as an NOP.

Input in Binary Mode If Ready (INA '0204). -- This instruction transmits the 6 least significant bits of the 8-bit ASR-33/35 character to the 6 least significant bits of the A-register. The A-register is not cleared. Ready must be honored within 1 ms to ensure transmission. If Ready is true, this instruction will be executed and the next instruction skipped. If Ready is not true, this instruction will be treated as an NOP.

Clear A and Input in ASCII Mode If Ready (INA '1004). -- Same as INA '0004 except A is cleared before character is transmitted.

Clear A and Input in Binary Mode If Ready (INA '1204). -- Same as INA '0204 except A is cleared before character is transmitted.

Output in ASCII Mode If Ready (OTA '0004). --This instruction transmits the 8 least significant bits of the A-register to the ASR-33/35. If the ASR-33/35 is punching, it will punch all 8 bits of the code that is transmitted. However, in printing, it will determine the character to be printed or the control function to be performed from the 7 least significant bits.

Output in Binary Mode If Ready (OTA '0204). -- This instruction transmits the 8 least significant bits of the A-register to the ASR-33/35 and then modifies channel 7 (normally A10) to be the inverse of A11. Thus, if the 8 least significant bits in the A-register were $(XX1XXXXX)_2$, they would be transmitted to the ASR-33/35 as $(X01XXXXX)_2$. If they were $(XX0XXXXX)_2$, they would be transmitted as $(X10XXXXX)_2$.

Set Interrupt Mask (SMK '0020). -- The A-register bit assignment for the ASR-33/35 is bit 11. This instruction sets the standard interrupt mask flip-flop if the A-register bit is ONE and resets the mask flip-flop if the bit is a ZERO.

Sample Program

The following subroutine is intended as an example only. When it is called, the subroutine will output one character to the ASR-33. The character will be printed if it is printable. If the punch is on, the character will be punched whether it is printable or not. The subroutine is entered with the character to be output in the A-register.

```
        REL
        SUBR    ASRTYP, STRT    Subroutine name
STRT    DAC     **              Subroutine entry point
        SKS     '104            Test ASR busy
        JMP     *-1             Delay until not busy
        OCP     '104            Enable output mode
        OTA     4               Output character in ASCII mode
        JMP     *-1             Delay if ASR not ready
        JMP     STRT            Return to calling program
        END
```

HIGH SPEED PAPER TAPE READER, MODEL 516-50

A high-speed, unidirectional perforated-tape reader is available as an option (DDP-516-50) which consists of a paper tape reader and the control logic that is required for operational compatibility. The reader employes a pinch roller capstan and brake solenoid system to control tape movement. The control logic includes an eight-bit buffer register the enables transfers via the I/O bus of one frame per computer. word. The reader reads eight data channels per frame at the rate of thirty inches per second. With a density of ten frames per inch, the rate is 300 frames per second.

Loading Procedure

The reader uses standard paper or mylar tapes (black paper recommended) 0.004 to 0.005 in. thick. The tape can be loaded without removing power by rotating a front-mounted READY-LOAD switch clockwise to the LOAD position. The tape must be placed with the three-channel side flush with the inboard guide. After the tape has been loaded, the READY-LOAD switch must be rotated counterclockwise to the READY position.

Programming

The reader operates continuously when reading is initiated with an OCP '0001. Data is transferred to the buffer until the complete tape has been read or until an OCP '0101 is executed.

The control codes assigned to the high-speed paper tape reader are described in the following paragraphs. In summary they are as follows.

OCP '0001	Start reader
OCP '0101	Stop reader
SKS '0001	Skip if tape reader ready
SKS '0401	Skip if tape reader not interrupting
INA '0001	Input from paper tape if ready
INA '1001	Clear A and input from paper tape if ready
SMK '0020	Set interrupt mask.

Start Reader (OCP '0001). -- This instruction starts tape motion. The first character to pass the read station is transferred to the device buffer for transmission to the central processor. An interval of 5 ms is required to reach full operating speed after execution of OCP '0001.

Stop Reader (OCP '0101). -- This instruction stops tape motion. This instruction must be executed within 1 ms after a character-ready signal to avoid losing the character after a restart.

Skip if Tape Reader Ready (SKS '0001). -- This instruction will skip if the tape reader is in a ready status. The tape reader is ready when a character is available in the device buffer.

Skip if Tape Reader Not Interrupting (SKS '0401). -- The tape reader is interrupting when a character is available and the interrupt mask flip-flop is set.

Input From Paper Tape Reader if Ready (INA '0001). -- Execution of this instruction causes a frame to be ORed into the eight least-significant bit positions of the A-register with channel 1 of the frame corresponding to bit position 16. The next program instruction is skipped upon execution of this instruction. If the Ready is not true, this instruction will be treated as an NOP.

Clear A and Input From Paper Tape Reader if Ready (INA '1001). -- This instruction is identical to INA '0001 except that the A-register is cleared before the character is transferred in.

Set Interrupt Mask (SMK '0020). -- The A-register bit assignment for the paper tape reader is bit 9. This instruction sets the standard interrupt mask flip-flop if the A-register bit is a ONE and resets the mask flip-flop if the bit is a ZERO.

Sample Program

The following subroutine is intended as an example only. When called, it will read two frames from the high-speed paper tape reader and pack the data read into one word. The packed word is left in the A-register upon return to the calling program.

```
        REL
        SUBR    PTR     Subroutine name
PTR     DAC     **      Subroutine entry point
        OCP     1       Start tape reader
        INA     '1001   Clear A and input first frame
        JMP     *-1     Delay until ready
        LGL     8       Shift to pack
        INA     1       Input second frame
        JMP     *-1     Delay until ready
        OCP     '101    Stop reader
        JMP*    PTR     Return
        END
```

Note in the above example that the tape reader was stopped in sufficient time to prevent loss of the following character.

HIGH-SPEED PAPER TAPE PUNCH, MODEL 516-52

The high-speed paper tape punch option (DDP-516-52) consists of a punch unit and the control logic required for interface with the DDP-516 computer. The punch is a synchronous device; pulses generated by a magnetic pickup coil synchronize the interface control circuits. The control logic includes an eight-bit buffer register that receives data transferred from the central processor. The device punches one-inch, eight-channel paper tape at the rate of 110 frames per second. (Oil impregnated tape is recommended.)

Loading Procedure

a. Thread tape off bottom rear of roll, through wire and roller guides, and then to tape guide and punch block.

b. Lead tape between hold-down bar and feed wheel, then out under tape cutter.

c. Apply punch power.

d. Depress feedout lever (located at top center of punch cover), pull the tape to the left until it begins to feed, and then release the feedout lever.

Programming

Punch power can be turned on by means of a switch on the device cabinet or under program control. A five second interval is required for the device to reach full operating speed after power has been applied. It is suggested that power only be applied under program control except during maintenance or replacement of tape supply.

The control codes assigned to the paper tape reader are described in the following paragraphs. In summary they are as follows.

OCP '0002	Enable paper tape punch
OCP '0102	Turn punch power off
SKS '0002	Skip if punch is ready
SKS '0102	Skip if punch power is on
SKS '0402	Skip if punch is not interrupting
OTA '0002	Output to punch if ready
SMK '0020	Set interrupt mask

Enable Paper Tape Punch (OCP '0002). -- This instruction applies power to the paper tape punch. There is a five-second delay until the punch is ready to receive data.

Turn Punch Power Off (OCP '0102). -- This instruction removes power from the paper tape punch. Ready status should be tested to be sure that it is Ready before execution of this instruction to avoid turning the punch off while data is being punched.

Skip if Punch is Ready (SKS '0002). -- This instruction will skip if ready status is true. Ready status is true when the device buffer is ready to accept new data from the central processor.

Skip if Punch Power is On (SKS '0102). -- This instruction must precede an OCP '0002. A character might be lost if an OCP '0002 is executed when power is already on.

Skip if Punch is Not Interrupting (SKS '0402). -- The punch is interrupting when the interrupt mask flip-flop is set and the buffer is ready to receive a character.

Output to Punch if Ready (OTA '0002). -- Execution of this instruction results in an output transfer. If Ready status is true, the eight least significant bits of the A-register are transferred to the device buffer and the next instruction is skipped. Ready status then becomes false for approximately 9 ms during which time the contents of the device buffer is punched as a frame, with channel 1 of the frame corresponding to bit position 16 of the A-register.

Set Interrupt Mask (SMK '0020). -- The A-register bit assignment for the Paper Tape Punch is bit 10. This instruction sets the standard interrupt mask flip-flop if the A-register bit is ONE and resets the mask flip-flop if the bit is ZERO.

Sample Program

The following subroutine is intended as an example only. When the subroutine is called, it will perform one of three functions depending on the entry used. The PON entry is used to apply power to the paper tape punch. It is a separate entry so that the calling program can perform other operations during the five-second interval required for the punch to reach full operating speed. The PNCH entry is used to punch an 80-character card image from a block of forty words packed two characters per word. The POFF entry is used after the last data block has been punched.

```
        REL
        SUBR    PON     Subroutine name for power-on
        SUBR    PNCH    Subroutine name for punch-data
        SUBR    POFF    Subroutine name for Power-off
PON     DAC     **      Power-on entry
        SKS     '102    Test power already on
        OCP     2       If not, turn on
        JMP*    PON     Return
PNCH    DAC     **      Punch-data entry
        LDA     =-40    Set CTR for 80 char. XFER
        STA     CTR     Store CTR
        LDA     BUFA    Get first loc. of block storage
        STA     LINK    Store in link
LOOP    LDA*    LINK    Get packed data word
        ICA             Set up left character
```

```
        OTA     2       Output character
        JMP     *-1     Delay if not ready
        ICA             Set up right character
        OTA     2       Output character
        JMP     *-1     Delay if not ready
        IRS     LINK    Increment storage address
        IRS     CTR     Increment CTR
        JMP     LOOP    Loop to punch next 2 characters
        JMP*    PNCH    Return
POFF    DAC     **      Power-off entry
        SKS     2       Test ready status
        JMP     *-1     Delay if not ready
        OCP     '102    Turn power off
        JMP*    POFF    Return
BUFA    DAC     COM     Address of packed word storage
LINK    BSS     1       Storage location counter
CTR     BSS     1       Word counter
COM     BSS     40      Packed word storage
        END
```

PARALLEL I/O CHANNELS, MODEL 516-32, 33, 34

Parallel I/O channels are the standard interface between the CPU and the I/O devices that can send and/or receive up to 16 bits of parallel data. There are three main options in this category as follows:

DDP-516-32	Parallel Input Channel
DDP-516-33	Parallel Output Channel
DDP-516-34	Buffered Parallel I/O Channel

A system may contain up to three parallel channels with any combination of the models listed above. These channels enable the computer to input data to and/or receive data from a device in any of the available modes of communication. Using the standard I/O bus, transfer rates are limited by the program speed or the speed of the device, whichever is less. With the DMC option, transfer rates up to 260 thousand words per second for input and 210 thousand words per second for output are possible. With the DMA option, transfer rates up to 460 thousand words per second for input and 320 thousand words per second for output are possible.

Programming

The following pages list and describe control codes used with parallel channels. The address and mask modifications that must be made to accommodate up to three I/O channels are as follows.

	Address	Mask Bit
First channel	30_8	5
Second channel	31_8	6
Third channel	32_8	7

The control codes given below are for the first channel, but are also applicable for the second and third channels providing the necessary change is made to the address.

Instruction Assignments

INA '0030	Input from parallel channel if ready
INA '1030	Clear A and input from parallel channel if ready
OTA '0030	Output to parallel channel if ready
OCP '0030	Enable input mode (516-32, 34)
OCP '0030	Enable output mode (516-33)

OCP '0130	Enable output mode (516-34)
OCP '0130	Device OCP 1 (516-32, 33)
OCP '0230	Device OCP 2 (516-32, 33, 34)
OCP '0330	Device OCP 3 (516-32, 33, 34)
OCP '0430	Device OCP 4 (516-33, 34)
OCP '0530	Device OCP 5 (516-34)
OCP '0630	Device OCP 6 (516-34 No DMC/DMA)
OCP '0630	Enable DMC/DMA mode (516-32, 33, 34)
OCP '0730	Reset DMC/DMA mode (516-32, 33, 34)
OCP '1630	Enable DMC/DMA Auto Switch Mode (516-32, 33, 34)
SKS '0030	Skip if channel ready
SKS '0130	Device SKS 1
SKS '0230	Skip if first DMC/DMA channel has not reached end-of-range
SKS '0330	Skip if not in Auto Switch Mode
SKS '0430	Skip if no interrupt request
SKS '0530	Device SKS 2
SKS '0630	Device SKS 3
SMK '0020	Set Interrupt Mask

Input from Paralle Channel if Ready (INA '0030). -- If the channel ready status flip-flop is not set, the program will execute the instruction following the INA. When the channel ready is set, the instruction will transfer 16 bits of data to the A-register, and the next sequential instruction will be skipped.

Clear A and Input from Parallel Channel if Ready (INA '1030). -- This instruction is identical to INA '0030 except that the A-register is cleared before the data is transferred.

Output to Parallel Channel (OTA '0030). -- This instruction transfers 16 bits of data from the A-register to the channel if the channel ready is set and skips the immediately following instruction. If ready is not set, the instruction is treated as an NOP.

Enable Input Mode (OCP '0030, DDP-516-32, 34). -- This OCP enables the parallel channel for data transfers in the input mode.

Enable Output Mode (OCP '0030, DDP-516-33; OCP '0130, DDP-516-34). -- These OCPs enable the parallel channel for data transfers in the output mode.

Device OCP Codes. --

Device OCP 1 (OCP '0130, DDP-516-32 and 33)
Device OCP 2 (OCP '0230, DDP-516-32, 33 and 34)
Device OCP 3 (OCP '0330, DDP-516-32, 33 and 34)
Device OCP 4 (OCP '0430, DDP-516-33 and 34)
Device OCP 5 (OCP '0530, DDP-516-34)
Device OCP 6 (OCP '0630, DDP-516-34) No DMC/DMA

These OCPs generate output pulses from the channel and may be utilized to control the device to which the channel is connected.

Enable DMC/DMA Mode (OCP '0630, DDP-516-32, 33, 34). -- This OCP enables the parallel channel in the DMC or DMA mode and resets the end-of-range interrupt. If not in the auto switch mode it selects channel 1.* It also resets the auto switch mode, and if not previously in the DMC/DMA mode, it resets the channel ready flip-flop.

Reset DMC/DMA Mode (OCP '0730, DDP-516-32, 33, 34). -- This OCP resets the parallel channel DMC/DMA mode, the end-of-range interrupt, and the end-of-transmission interrupt. It also resets the DMC/DMA auto switch mode and selects channel 1.*

Enable DMC/DMA Auto Switch Mode (OCP '1630, DDP-516-32, 33, 34). -- This OCP enables the DMC/DMA auto switch mode for the parallel channel, resets the end-of-range interrupt, and selects channel 1* if not already in the auto switch mode.

Skip if Channel Ready (SKS '0030). -- This instruction will cause the next instruction in the program to be skipped if the channel "Ready" flip-flop is set.

Device SKS 1 (SKS '0130). -- This instruction will test the state of the device sense line (SKS 01-). If it is a logic zero (+6V) the next instruction in the program will be skipped, if a logic one (ground) the next instruction will be executed.

Skip if First DMC/DMA Channel has not Reached End-of-Range (SKS '0230). -- This instruction will cause a skip of the next instruction in the program if Auto Switch is installed and DMC/DMA Channel 1 has not reached End-of-Range.

Skip if Not Auto Switch Mode (SKS ' 0330). -- This instruction will cause the next instruction in the program to be skipped if parallel input channel is not in Auto Switch mode.

*Channel 1 refers to one of the two DMC/DMA channels required for Auto Switch operation. (Channel 1 = one DMC/DMA channel and Channel 2 = another DMC/DMA channel.

Skip if No Interrupt Request (SKS '0430). -- This instruction will cause the next instruction in the program to be skipped if parallel input channel is not generating a standard interrupt request.

Device SKS 2 (SKS '0530). -- Same as SKS 1 except for line SKS02-.

Device SKS 3 (SKS '0630). -- Same as SKS 1 except for line SKS03-.

Set Mask (SMK '0020). --

$(A)_5$	Mask flip-flop (channel 1)
$(A)_6$	Mask flip-flop (channel 2)
$(A)_7$	Mask flip-flop (channel 3)

NOTE

Proper selection of the interrupt mode requires that an input or output mode has been enabled prior to execution of SMK '0020.

DMC/DMA Mode Selection

The following sequence is required to select DMC or DMA mode (depending on which bus is connected to the channel).

a. Establish starting and ending addresses
b. OCP '0630 to enable mode
c. SMK01 with A-register bit 5, 6, or 7 set to 1
d. OCP '0030 or OCP '0130

Selection of DMC/DMA auto switch mode is the same sequence as described above except that an OCP '1630 must follow immediately the OCP '0630.

DMC/DMA End of Range

After the parallel channel has executed the required number of transfers, it stops executing DMC/DMA transfers but remains in the DMC/DMA mode. If additional data transfers are desired, the new starting address and range should be established and followed by an OCP '0630.

NOTE

With the DDP-516-34 option, if additional transfers in the opposite direction are desired, an OCP '0030 or OCP '0130 should be issued before the OCP '0630.

If termination is desired, an SMK01 (with the A-register bit 5 equal to zero) and an OCP '0730, respectively, must be executed.

DMC/DMA End of Transmission

A stop transmission interrupt can be reset with an OCP '0730.

DMC/DMA Auto Switch End of Range

The parallel channel continues operating in the auto switch mode after an end-of-range. An OCP '0630 must be issued to terminate the auto switch mode. Transfers will terminate when the next end-of-range occurs.

SKS/OCP OPTION, MODEL 516-29

The SKS/OCP option adds 16 OCP and 16 SKS instructions to a system's OCP and SKS capability. The OCP instructions can be used to control 16 different functions. The SKS instructions can be used to test the status of 16 discrete lines.

Operation

The 16 SKS lines can be tested with an unique SKS instruction. If the state of a line is a logic ONE (+6V), the program will skip the next instruction; if logic ZERO (ground), the next instruction is executed.

The 16 OCP lines are controlled by 16 unique OCP instructions, each of which can be used to control a different function. Execution of an OCP puts a negative (ground) pulse on the addressed OCP line. This pulse is a minimum of 525 ns and a maximum of 1425 ns in width.

Programming

This option looks like a "device" on the I/O bus -- its device address is 34_8. The function bits of the SKS and OCP instructions are decoded to provide the 16 different SKS's and OCP's.

The following instructions are included. Each takes two cycles.

```
OCP '0034          SKS '0034
OCP '0134          SKS '0134
OCP '0234          SKS '0234
     '                  '
     '                  '
     '                  '
     '                  '
OCP '1734          SKS '1734
```

CARD READER, MODEL 516-61

The Card Reader Option (DDP-516-61) includes a 200-cpm card reader and a card reader control unit (CRCU) that contain appropriate interface logic to ensure DDP-516 operational compatibility. The card reader is a photoelectric device that reads Hollerith or binary-coded punched cards, one at a time, column-by-column, and transmits the data read to the DDP-516 interface.

In the Hollerith mode the card reader reads each column as a Hollerith character and converts it to a six-bit code (see Table 5-2). The converted characters are then transmitted to the DDP-516 interface as bits 11 through 16 of the data word.

In the binary mode the card reader reads each column as a 12-bit byte. Data are transferred to the DDP-516 interface in bit positions 5 through 16 of the data word, with bit position 5 represented by row 12 and bit position 16 represented by row 9. This action continues for each column up to and including column 80.

Programming

The control codes assigned to the card reader are as follows.

OCP '0005	Read one Hollerith card
OCP '0105	Read one binary card
SKS '0005	Skip if card reader ready
SKS '0105	Skip if card reader not busy
SKS '0205	Skip if not end of file
SKS '0305	Skip if card reader operational
SKS '0405	Skip if card reader not interrupting
INA '0005	Input from card reader if ready
INA '1005	Clear A-register and input from card reader if ready
SMK '0020	Set interrupt mask.

Read One Hollerith Card (OCP '0005). -- This OCP causes the card reader to feed one card and enables 6-bit Hollerith encoded characters to be read into the A-register with an INA 'X005 instruction.

Read One Binary Card (OCP '0105). -- This OCP causes the card reader to feed one card and allows 12-bit binary data to be read into the A-register with an INA 'X005 instruction.

NOTE

Proper operation of the system is not guaranteed if these OCP's are issued when the card reader is busy.

Skip if Card Reader Ready (SKS '0005). -- This SKS will skip if the control unit is ready to send a character to the input bus. The first ready will occur approximately 110 ms after an OCP read instruction is received. Subsequent readys occur every 2.4 ms.

Skip if Card Reader Not Busy (SKS '0105). -- This SKS will skip if the card reader is not busy. The card reader is busy from the time OCP '0005 or OCP '0105 is received until 1 ms after the 80th column of the card has been read (a total duration of approximately 300 ms).

Table 5-2.
Card Codes

Octal ⚠1	Card (Hollerith)	Character	Octal	Card (Hollerith)	Character
00	All Other Codes		40	11	-
01	1	1	41	11-1	J
02	2	2	42	1-2	K
03	3	3	43	11-3	L
04	4	4	44	11-4	M
05	5	5	45	11-5	N
06	6	6	46	11-6	O
07	7	7	47	11-7	P
10	8	8	50	11-8	Q
11	9	9	51	11-9	R
00	0	0	52	11-8-2	;
13	8-3	=	53	11-8-3	$
14	8-4	,	54	11-8-4	*
15	8-5	:	55	11-8-5	[
16	8-6	!	56	11-8-6	End-of-File
17	8-7	>	57	11-8-7	<
20	Blank	Space	60	12	+
21	0-1	/	61	12-1	A
22	0-2	S	62	12-2	B
23	0-3	T	63	12-3	C
24	0-4	U	64	12-4	D
25	0-5	V	65	12-5	E
26	0-6	W	66	12-6	F
27	0-7	X	67	12-7	G
30	0-8	Y	70	12-8	H
31	0-9	Z	71	12-9	I
32	0-8-2		72	12-8-2	↑
33	0-8-3	,	73	12-8-3	.
34	0-8-4	(	74	12-8-4	)
35	0-8-5		75	12-8-5	%
36	0-8-6	]	76	12-8-6	\
37	0-8-7	"	77	12-8-7	←

⚠1 Octal column is 6-bit code generated by card reader.

Skip if Not End-of-File (SKS '0205). -- This SKS will skip if the end-of-file flip-flop is not set. The EOF flip-flop is set by an 11-8-6 punch read in Hollerith mode or by pushing the END OF FILE button on the reader console when the input hopper is empty. It is reset every time a read card OCP is issued or on master clear.

Skip If Card Reader Operational (SKS '0305). -- This SKS will skip if the card reader is in an operational state (that is, power on, feed hopper not empty, no card jam, stacker not full, no read-feed or validity errors, and start button depressed). The level indicating that the card reader is not operational cannot be reset by MASTER CLEAR. If it was set by READ CHECK, FEED CHECK or VALIDITY CHECK, which will be indicated by the fact that the particular light on the reader console will be on, both the RESET and START buttons have to be pushed in order to reset the level. If it was set by any other condition (input hopper empty or output stacker full), correcting the condition and depressing the START button will reset the level. In all the above cases, if the condition which caused the fault in the first place is still present, the level cannot be reset. If a read OCP is issued when the card reader is not operational the CRCU will become busy but no card will be clutched. If the non-operational status was caused by an empty input hopper, some programs may be resumed by placing cards in the hopper and depressing the START button.

Skip If Card Reader Not Interrupting (SKS '0405). -- This SKS will skip if the card reader has not caused an interrupt. This SKS is used when operating with standard interrupt to determine which device is ready to send or receive new data.

Input from Card Reader If Ready (INA '0005). -- If the control unit is not ready to transfer data the INA is treated as a NOP and the program will continue in sequence. When the control unit ready flip-flop has been set data is transferred to the A-register in the following manner and the next instruction is skipped.

Hollerith Mode. -- The card reader 6-bit output is ORed into the A-register bit positions 11 through 16. Bits 1 through 10 are unchanged. Card reader codes are listed in Table 5-2.

Binary Mode. -- The 12 bits from one card column, rows 12 through 9, are ORed into A-register bit positions 5 through 16. Bits 1 through 4 are unchanged. The device must be serviced within 2.4 ms after a ready signal is received to ensure that each column of data is successfully transferred.

Clear A-Register and Input from Card Reader If Ready (INA '1005). -- This instruction is identical to INA '0005 but the A-register is cleared before data is transferred.

Set Interrupt Mask (SMK '0020). -- The A-register bit assignment for the Card Reader is bit 12. This instruction sets the standard interrupt mask flip-flop if the A-register bit is a ONE and resets the mask flip-flop if the bit is a ZERO.

Operator Controls and Indicators

Pushbutton combination switches and lamps to indicate the status of the card reader are located on the card reader control panel. Front panel controls and indicators are as follows:

Controls	Function
POWER ON	Applies ac power to reader controls and logic.
POWER OFF	Turns off ac power to reader.
START	Sends a ready level to card reader interface, signalling that a read cycle may commence.
STOP	Stops card reader operation.
RESET	Resets all error condition signals except the NOT READY indicator (this signal can only be reset when the start pushbutton is depressed).
END OF FILE	Selects end of file status and signals card reader interface logic.
VALIDITY ON	Selects validity checking logic. (Hollerith mode only)
NOT READY	Indicates that card reader is not ready to begin reading operating when when indicator is lit.
READ CHECK	Indicates that one of the photocell exciter lamps is not on or is blocked.

NOTE

READ CHECK does not mean that a card was read incorrectly. This light cannot be energized while a card is actually passing through the read station. It can be set while no cards are in motion, before a card has entered the read station, or after it has left the read station.

FEED CHECK	Indicates a card jam or that a card has failed to feed (did not reach the read station).
VALIDITY CHECK	Indicates that a code other than a legitimate Hollerith code was read while in the Hollerith mode and with the VALIDITY ON switch energized. All illegal codes will be input to the computer as octal 00.

Placement of Cards in Hopper

The card reader accepts standard 7-3/8 in. by 3-1/4 in. punch cards 0.0070 in. thick. Cards should be placed in the hopper face down with the row-9 edge toward the back of the card reader.

Sample Program

The following subroutine is intended as an example only. When it is called, it will read Hollerith data from a card and pack it two-characters per word for a maximum of

40 words. To keep the example simple, no provision has been made to convert from the 6-bit Hollerith code to the 8-bit ASCII code.

```
         REL
         SUBR    CARD        Subroutine name
CARD     DAC     **          Subroutine entry name
         LDX     =-40        Set index for 80 char. XFER
         SKS     '305        Test card reader operational
         JMP     *-1         Delay until operational
         SKS     '105        Test card reader busy
         JMP     *-1         Delay until not busy
         OCP     '5          Read one Hollerith card
         INA     '1005       Clear A and Input character
         JMP     *-1         Delay if not ready
         ICR                 Shift to pack
STRT     INA     '5          Input character
         JMP     *-1         Delay if not ready
         STA*    BUF+40,1    Store word
         IRS     0           Increment index
         JMP     STRT        Loop to read next two char.
         JMP*    CARD        Return
         BSS     40          Packed word storage
         END     CARD        End of subroutine
CARD     SUBR    CARD
                             Return
BUFA     DAC     COM         Address of packed word storage
LINK     BSS     1           Storage location counter
CTR      BSS     1           Word counter
COM      BSS     40          Packed word storage
         END     CARD        End of subroutine
```

LINE PRINTER, MODEL 516-7050

The Line Printer Option (DDP-516-7050) consists of an Anelex 4000 Series Unbuffered Shuttle Line Printer and a line printer control unit that provides appropriate interface to ensure operational compatibility. Nominal output printing speed of the 64-character set with single line spacing is 300 lpm.

The printer operates by means of a rotating character drum, a bank of 60 print hammers, and a character code disc that is fixed to one end of the drum. The paper and inked ribbon are between the hammers and the drum. Around the drum are 64 different characters, including capital letters, digits, and commonly used symbols (See Table 5-3). Each character is repeated 60 times across the drum, at the positions of the print hammers, but skewed slightly in the direction of rotation, and the DDP code for each character is engraved on the code disc at the angular position corresponding to each character row.

Two revolutions of the character drum are required to print each 120-character line. The characters at the odd- (or even-) numbered positions on the paper are printed during the first revolution. The paper then is shifted (shuttled) one character position to the left (or right), and the characters at the even- (or odd-) numbered positions are printed during the second revolution.

The line-printer paper-advance mechanism is controlled by a dual-channel paper tape loop. Normally one channel controls spacing to top of form, and the other controls normal line spacing. However, the loop can be punched to control any spacing desired.

Data Format

A 120-character line of data must be formatted into a 60-word block of memory prior to output. Each word contains two 6-bit characters with the odd character in bit positions 3-8 and the even character in bit positions 11-16. The first two bits of each half word are not interpreted and can be the high order bits of ASCII characters. Thus:

Column	1	2	3	4		119	120
	00XXXXXX	00XXXXXX	00XXXXXX	00XXXXXX	-----	00XXXXXX	00XXXXXX
Word	1		2			60	

Table 5-3
Line-Printer Characters

Character Printed	DDP-516 Octal Code	Character Printed	DDP-516 Octal Code
Blank	40	@	00
!	41	A	01
"	42	B	02
#	43	C	03
$	44	D	04
%	45	E	05
&	46	F	06
'	47	G	07
(	50	H	10
)	51	I	11
*	52	J	12
+	53	K	13
,	54	L	14
—	55	M	15
.	56	N	16
/	57	O	17
0	60	P	20
1	61	Q	21
2	62	R	22
3	63	S	23
4	64	T	24
5	65	U	25
6	66	V	26
7	67	W	27
8	70	X	30
9	71	Y	31
:	72	Z	32
;	73	[	33
<	74	/	34
=	75	]	35
>	76	↑	36
?	77	←	37

Scanning

The printer is "unbuffered" in that it uses computer memory for storage of a complete line. The computer must output each word in the print area sequentially for every character in the print set. For example, the 60 words should be outputted to print all the "As", then the 60 words would be outputted again to print all the "Bs", etc. Each pass through the 60-word print area is called a scan. As there are 64 different characters in the character set, 64 scans might have to be made to print the 60 odd or even halves of a line. As many scans are made as are necessary so the total number of hammers fired plus spaces counted equal 60.

Shuttling

As soon as all 60 hammers (or spaces) have been fired, shuttling takes place automatically. No computer-issued OCP is necessary to initiate the shuttle operation. When the shuttling is complete (20 ms), up to 64 scans are made for the other half of the line.

Paper Advance

Paper advance is initiated by computer command (OCP) and controlled by a paper tape format loop. There are two channels on this loop; Channel 1 for top of form and Channel 2 for single space.

Timing (See Figure 5-2)

Scans occur every 1.25 milliseconds during the printing of an odd or even half line. The 64 scans required for half a line thus take 80 ms (64 x 1.25). Shuttle and paper advance (single-space) each take approximately 20 ms, for a total line time of 200 ms (300 lpm).

The printer requires that a scan (outputting of 60 words) takes place within 840 μsec, leaving 410 μsec between each scan. During the 840 μsec scan, 60 words must be outputted, which is an average of a word every 14 μsec. To accommodate DMC operation, "ready" comes up every 28 μsec, during which time two words must be outputted.

Computer Utilization

In the I/O bus mode of operation, the computer can be used for other programmed operations during shuttle and paper advance time. Both of these operations can cause an interrupt when complete. Thus, programming (calculations, formatting, etc.) can occur 40 ms out of each 200 ms print cycle.

When in either DMC or DMA operation, each word outputted will cause a break in the program concurrently being executed. Address and range must be re-established for each scan. End-of-scan as well as paper advance complete can cause an interrupt when in either DMC or DMA Mode.

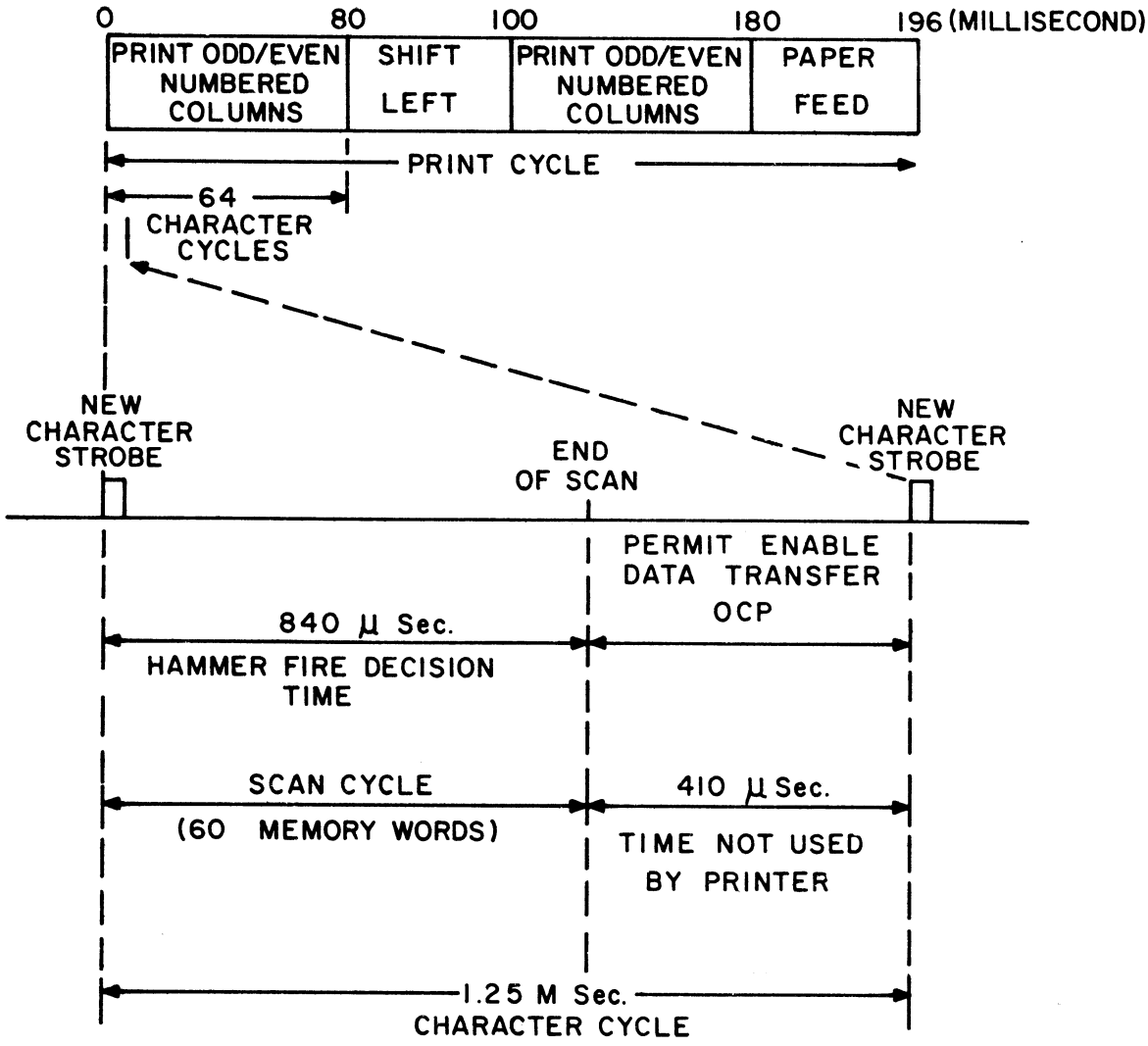


Figure 5-2. Line Printer - Print and Character Cycles

Approximations for CPU time utilized are as follows:

Mode	% Time Utilized	% Time Free
I/O Bus	80%	20%
DMC	18%	82%
DMA	8%	92%

Instructions

The line printer has a device address of $(03)_8$, and a mask bit assignment (SMK) of Bit 14 in the A-register. The instructions assigned to the line printer are described on the following pages. In summary, they are as follows:

OCP '0003	No paper advance
OCP '0203	Advance paper to channel 2
OCP '0303	Allow memory scan via DMA/DMC
OCP '0403	Advance paper to channel 1
OCP '0703	Enable memory scan via the I/O bus
SKS '0003	Skip if ready
SKS '0203	Skip if no alarm
SKS '0303	Skip if odd column next
SKS '0403	Skip if not interrupting
SKS '1103	Skip if line is printed
SKS '1203	Skip if not shuttling
SKS '1303	Skip if line is printed and not shuttling
SKS '1403	Skip if not advancing paper
SKS '1503	Skip if line is printed and not advancing paper
SKS '1603	Skip if not shuttling and not advancing paper
SKS '1703	Skip if not busy
OTA '0003	Output to line printer is ready
SMK '0020	Set interrupt mask

No Paper Advance (OCP '0003). -- This OCP initializes the interface logic without advancing the paper to a new line. It can be used to overprint a line.

Advance Paper to Channel 2 (OCP '0203). -- This OCP advances the paper under control of channel 2 on the paper tape format loop (normally used to advance paper one line).

Allow Data Transfer Via DMA/DMC (OCP '0303). -- This OCP enables the transfer of words from the central processor to the printer by way of the DMA or DMC channels. When end-of-range is reached, the DMA/DMC subchannel becomes inactive and requests service with an interrupt.

Advance Paper to Channel 1 (OCP '0403). -- This OCP advances the paper under control of channel 1 on the paper tape format loop (normally used to advance paper to the top of the next page).

Enable Memory Scan Via I/O Bus (OCP '0703). -- This OCP enables transfer of words from the central processor to the printer via the standard I/O bus.

One of the paper tape advance OCPs ('0003, '0203, or '0403) must be issued after each complete line is printed if it is desired to continue printing. (The printing of a line can be tested with an SKS '1103.)

If OCP '0203 or '0403 is issued during shuttle time, the next 60 characters will be printed in their proper positions but on adifferent line than the first 60 characters. If OCP '0003 is issued during shuttle time, it will have no effect on printer operation. (Shuttle time can be tested with an SKS '1203.)

One of the enable OCPs ('0303 or '0703) is required for a memory scan to take place (contents of memory locations transferred to printer for comparison). Each Data Transfer OCP required to complete printing half a line subsequent to the first OCP must be issued not less than X ns, but not more than 410 ns, after the end of scan; where X is defined as 21 ns from the next to last OTA of a scan in the I/O bus mode, and 14 ns from end-of-range in DMC/DMA mode (see Figure 5-2). Operation of the printer is undefined if either of these OCPs is issued at any time other than that shown in Figure 5-2. Any of the OCPs will acknowledge the standard interrupt (see SKS '0403).

Skip if Ready (SKS '0003). -- This SKS tests the status of the channel ready flip-flop to determine whether the printer is ready for a data transfer.

Skip if No Alarm (SKS '0203). -- This SKS tests the alarm status that can be caused by any one of the following conditions:

a. Device failures:
   (1) Printer power supplies over/under voltage
   (2) Hammer fuse blown
   (3) S-Pac power supply failure
   (4) Hammer cable not in place
   (5) S-Pac hammer amplifiers missing
b. Incorrect shuttle operation
c. Printer yoke open
d. Printer power failure
e. No paper in printer
f. Lack of response by the computer to printer data transfer request

Any printer OCP will attempt to reset the alarm. Conditions a through e will not reset unless corrected. Condition f indicates that the line should be overprinted or printed again.

Skip if Odd Column Next (SKS '0303). -- This SKS tests whether the paper is currently shifted left or right, and may be used anytime except when a shuttle operation is in progress. The next instruction will be skipped if the paper is shifted right. This test is not required for proper operation.

Skip if Not Interrupting (SKS '0403). -- This SKS tests the interrupt status that normally can be caused by any one of the following conditions:

a. Mask set, DMA/DMC mode set, and end of range
b. Mask set and paper feed complete in either the standard I/O mode or the DMA/DMC mode
c. Mask set, standard I/O mode set, and shuttle complete.

Skip if Line is Printed (SKS '1103). -- This SKS will skip if the line printed status is set. The line printed status is true after all 120 characters (including spaces) have been printed, and remains true until an enable data transfer OCP has been issued. The line printed status will also be true when the printer is master cleared.

Skip if Not Shuttling (SKS '1203). -- This SKS tests whether the printer is in the process of shuttling the paper. The shuttling signal remains true for a maximum of 21.5 ms after the 60th character (including spaces) of the first half of a line has been printed.

Skip if Line is Printed and Not Shuttling (SKS '1303). -- This SKS is a combination of SKS '1103 and SKS '1203.

Skip if Not Advancing Paper (SKS '1403). -- A maximum of 17 ms is required to advance paper for a single line feed. To advance paper to top-of-form, 16 + (n - 1)(6.67) ms is required (where n is the number of lines skipped to reach top-of-form). For multiple line spacing other than top-of-form (i.e., two or more successive OCP '0203 without printing in between) 36 ms for each OCP after the first one is required.

Skip if Line is Printed and Not Advancing Paper (SKS '1503). -- This SKS is a combination of SKS '1103 and SKS '1403.

Skip if Not Shuttling and Not Advancing Paper (SKS '1603). -- This SKS is a combination of SKS '1203 and SKS '1403.

Skip if Not Busy (SKS '1703). -- Not busy is defined as line printed, printer not shuttling, and printer not advancing paper.

Output to Printer (OTA '0003). -- This instruction transfers a data word from the A-register to the line printer via the output bus. The proper half of the 16-bit word is determined by the hardware for the odd or even column printing.

Set Interrupt Mask (SMK '0020). -- The A-register bit assignment for the line printer is bit 14. This instruction sets the standard interrupt mask flip-flop if the bit is a ONE and resets the mask flip-flop if the bit is a ZERO.

Program Timing

When the printer has been enabled for a scan cycle (by an OCP '0303 or an OCP '0703) a ready status is entered when the printer sends a new character signal to the interface. The ready status indicates to the central processor that two output words are being requested. Transmission of the second output word from the central processor then resets the ready status. A ready signal is generated every 28 μ sec after the first ready signal.

Standard I/O Bus. -- Ready signals are generated until the memory scan is complete (60 output words). An alarm status results if the two output words are not received by the printer interface within 19 μ sec after the ready signal was generated. If this occurs, it is still possible to overprint a line by using an OCP '0003 (no paper advance) and an OCP '0703 (enable I/O bus). Execution of instructions other than those for servicing the printer should not be allowed concurrently with printer operations when using the standard I/O bus. Execution of other instructions would cause cumulative delays between OTA instructions for the printer and could result in an alarm status on every memory scan.

DMC Option. -- Ready signals are generated every 28 μ sec until end-of-range is reached. The DMC range should be set for 60 words for proper operation. An alarm status results if two output words are not received by the printer interface with 19 μ sec after each ready signal is generated. (The limiting factor for T_{wc} in the discussion of DMC in Section IV is 19μsec.)

DMA Option. -- An alarm status results if the first output word is not received by the printer interface within 19 μ sec after the ready signal was generated. (If this should occur, it is a symptom of a system overload rather than a violation of a programming constraint.)

Operator Controls and Indicators

Switches and lamps located on the operator control panel are as follows:

Control/Indicator	Function
ON pushbutton switch/lamp	Initiates power-on sequence and indicates that power is on.
OFF pushbutton switch/lamp	Initiates power-off sequence and indicates that power is off.
ALARM STATUS lamp	Indicates a non-operating device.
SHUTTLE switch	Shuttles paper to left or right depending on present position of paper.

YOKE OPEN lamp	Indicates that the yoke has been left open.
START lamp	Indicates no alarm status, yoke not open, power on, paper remaining, and correct shuttle position.
TOP OF FORM switch	Advances paper until a hole is detected in channel 1 of the vertical format tape.
SINGLE SPACE switch	Advances paper until a hole is detected in channel 2 of the vertical format tape.

Sample Program

The following subroutine is intended as an example only. When called, it will print one line on the line printer and advance the paper. If an alarm condition exists upon entry, an alarm flag is set and control is returned to the calling program.

```
            REL
            SUBR    PRNT        Subroutine name

PRNT        DAC     **          Entry point
            SKS     '1703       Delay if printer busy
            JMP     *-1
SCAN        LDX     =-60        Set index for 60-word transfer
            OCP     '703        Enable scan
CONT        LDA     BUF+60,1    Get data word
            SKS     '203        Test for alarm condition
            JMP     ERR         Go process alarm (undefined in example)
            OTA     3           Output word
            JMP     *-3         If printer not ready check for alarm
            IRS     0           Update index
            JMP     CONT        If scan incomplete, continue
            SKS     '1203       Is shuttling taking place
            JMP     *-1         Yes 1/2 line is printed, wait for shuttle complete
            SKS     '1103       Check for line complete
            JMP     SCAN        Line incomplete, scan again
            OCP     '203        Line complete, advance paper
            JMP*    PRNT        Return

BUF         BSS     60          Line to be printed
```

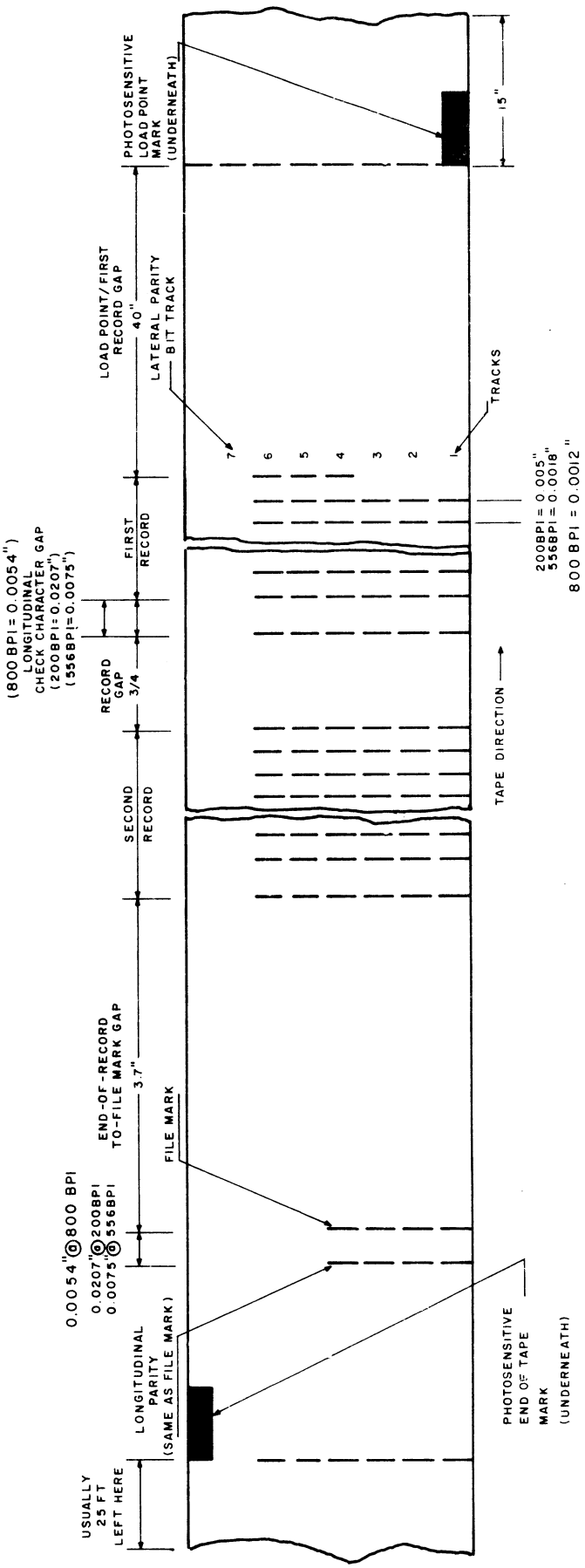


Figure 5-3. Magnetic Tape Format

MAGNETIC TAPE SYSTEMS, MODEL 4100

A DDP-516 Magnetic Tape System can include either one or two tape control units (TCUs), each controlling up to four tape transports. Six types of tape transports are available. These consist of 36- and 80-inch-per-second models operable at recording densities of 200 and 556, 200 and 800, or 556 and 800 bits-per-inch. Any system can be connected to the computer via the I/O bus or the DMA bus. Provision is also made for a DMC subchannel.

Tape Format

Figure 5-3 shows how data is organized into records and files on tape. Six data tracks and one parity track are used to record standard IBM tape recording characters as shown. A record may contain any number of six-bit characters with one character per frame. Track 7 of each frame is used for parity. Even parity is indicated by an even number of bits in a given frame (including Track 7). Odd parity is just the opposite of even parity.

Information can be written and read in three modes: two characters-per-word BCD, two characters-per-word binary, and three characters-per-word binary. Figure 5-4 shows the correspondence between a word in the A-register and the frames recorded on tape for each mode. Even parity is used in the BCD mode and odd parity is used in the binary modes. In either mode longitudinal even parity is indicated for each track at the end of a record. Since the file mark (17_8) is a single frame record, the file mark longitudinal parity frame is identical to the file mark itself.

To accomplish IBM tape code compatibility in the BCD mode of operation, the octal value 00 is converted to the octal value 12 when writing. Conversely, when reading, the octal value 12 is converted to the octal value 00. No other code conversion is performed automatically.

Programming

The control code assigned to the magnetic tape options are described on the following pages. The value of X should be selected from 0 to 7 to complete the particular tape transport address as shown in Table 5-4.

Table 5-4.
Tape Transport Addresses

MTT	TCU No. 1 MTT Addresses	TCU No. 2 MTT Addresses
1	10	14
2	11	15
3	12	16
4	13	17

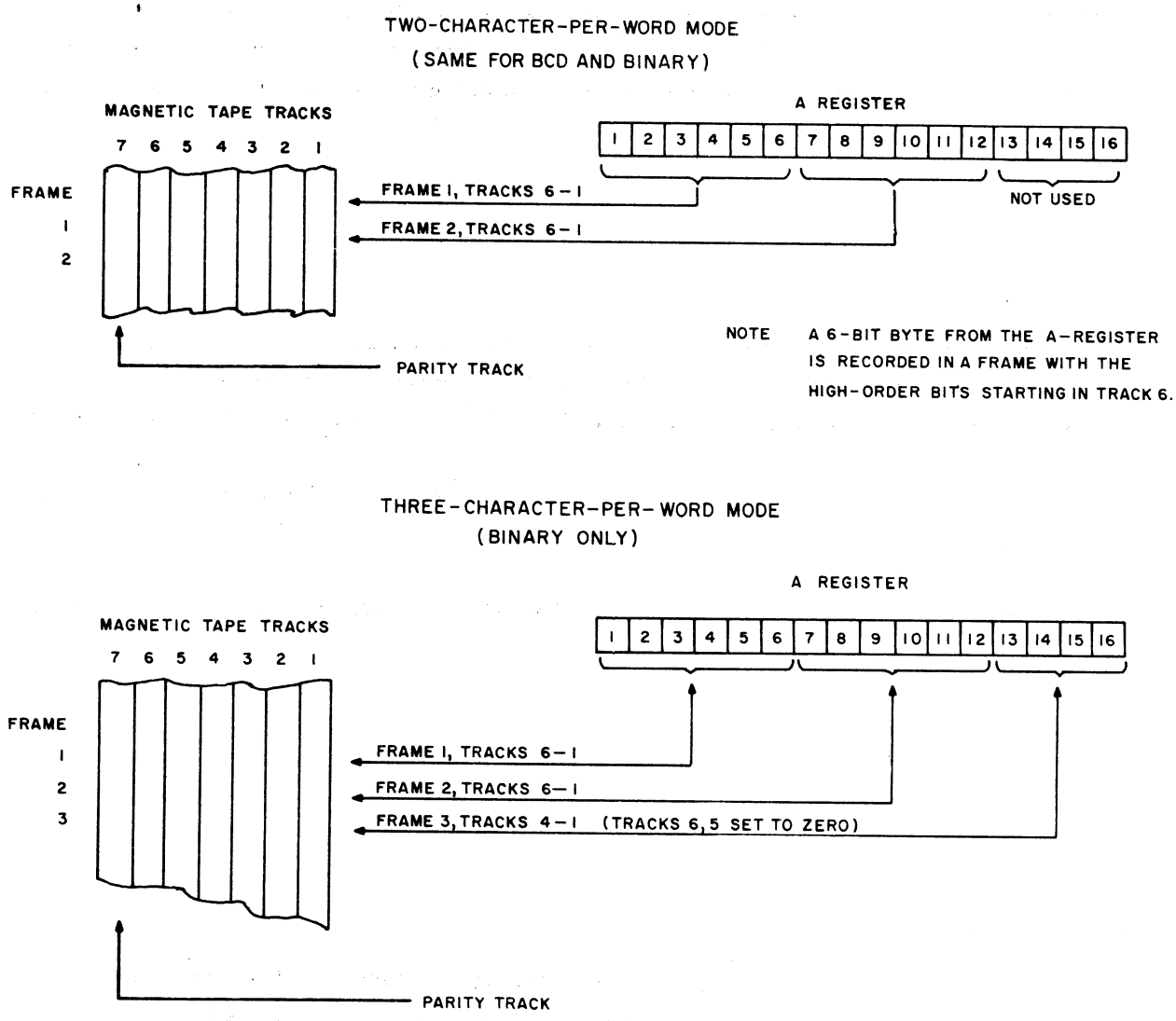


Figure 5-4. Correspondence between the A-Register Word and Tape Format

OCP '001X	Read BCD, 2 characters per word
OCP '011X	Read binary, 2 characters per word
OCP '021X	Read binary, 3 characters per word
OCP '031X	Set up normal DMC/DMA mode
OCP '041X	Write BCD, 2 characters per word
OCP '051X	Write binary, 2 characters per word
OCP '061X	Write end of file
OCP '071X	Reset DMC/DMA mode
OCP '101X	Write binary, 3 characters per word
OCP '111X	Space forward one record
OCP '121X	Space forward one file
OCP '131X	Set up DMC/DMA in auto switch mode
OCP '141X	Rewind
OCP '151X	Backspace one record
OCP '161X	Backspace one file
OCP '171X	Stop write
SKS '001X	Skip if ready
SKS '011X	Skip if not busy
SKS '021X	Skip if an error has not be detected
SKS '031X	Skip if not at beginning of tape (loadpoint)
SKS '041X	Skip if not interrupting
SKS '051X	Skip if end of tape has not been detected
SKS '061X	Skip if end of file has not been detected
SKS '071X	Skip if writing is permitted
SKS '111X	Skip if MTT operational
SKS '121X	Skip if DMA/DMC subchannel is not currently processing Channel No. 2
SKS '131X	Skip if DMC/DMA subchannel is not auto switch mode
SKS '141X	Skip if not rewinding
INA '001X	Input from TCU if ready
INA '101X	Clear A-register and input from TCU if ready
OTA '001X	Output data to the TCU
SMK '0020	Set TCU interrupt mask.

NOTE

OCP '031X, '071X, '131X, and '171X are not MTT action commands, but will affect MTT selection. All OCP's except these are interlocked with the TCU BUSY signal.

All SKS instructions except rewind apply to the last selected transport, and are associated with the TCU (they ignore address bits 15 and 16). Rewind SKS is associated with a transport and may be checked anytime.

Read BCD, 2 Characters per Word (OCP '001X). -- This instruction initiates a BCD record transfer. It conditions the word-forming buffer to accept BCD data and to pack two characters per word. Transverse parity is even and a code conversion is performed for zero. Upon receipt of this instruction the TCU executes a forward command to the selected transport and motion continues until a no-data gap is reached following a data field.

Read Binary, 2 characters per word (OCP '011X). -- This instruction initiates a binary record transfer. It conditions the word-forming buffer to accept binary data and to pack two characters per word. Transverse parity is odd and there is no character conversion. Upon receipt of the OCP, the TCU executes a forward command to the selected transport and forward motion continues until a no-data gap is reached following a data field.

Read Binary, 3 Characters per Word (OCP '021X). -- This instruction initiates a binary record transfer. The word-forming buffer is conditioned to accept binary data and to pack three characters per word. Transverse parity is odd and there is no character code conversion. (This read mode is used to read tapes prepared on 16-bit compatible systems due to the word construction.) This OCP causes forward motion that continues until a no-data gap is reached following a data field.

Set Up Normal DMC/DMA Mode (OCP '031X). -- This instruction prepares for record transfers utilizing the DMC or DMA mode if the TCU is so equipped. It conditions the DMC/DMA subchannel but does not execute any commands to the transport. It also resets the end of range flip-flop.

Write BCD, 2 Characters per Word (OCP '041X). -- This OCP instruction initiates a BCD record transfer. Upon receipt of this instruction, the word-forming buffer is initialized and is ready to receive data from the CPU and to unpack two characters per word. The TCU executes a forward command to the transport and motion continues until the program fails to successively honor the buffer-ready status causing subsequent read-after-write record gap detection. Even transverse parity is generated by the TCU.

Write Binary, 2 Characters per Word (OCP '051X). -- This instruction initiates a binary record transfer and causes the word-forming buffer to initialize and be ready to receive data immediately from the CPU and to unpack two characters per word. The TCU executes a forward command to the transport and motion continues until the program fails to honor the buffer-ready status, causing subsequent read-after-write record gap detection. Odd transverse parity is generated by the TCU.

Write End of File (OCP '061X). -- Execution of this instruction applies a forward command to the selected transport. After the appropriate delay during which the proper gap is formed, the TCU writes a file mark and a file mark longitudinal parity character on the tape. Forward motion then continues until the TCU reads the file mark just written and sets the end of file status.

Reset DMC/DMA Mode (OCP '071X). -- This instruction disables DMC or DMA mode of transfers in the TCU and resets the end-of-range-interrupt control flip-flop, the external-stop control flip-flop, the channel ID storage flip-flop, and the auto-switch mode flip-flop.

Write Binary, 3 Characters per Word (OCP '101X). -- This OCP instruction initiates a binary record transfer. It initializes the word-forming buffer so that it is ready to receive data from the CPU and to unpack three characters per word. The TCU executes a forward command to the transport, and motion continues until the program fails to honor the buffer-ready status, causing subsequent read-after-write record gap detection. Odd transverse parity is generated by the TCU.

Space Forward One Record (OCP '111X). -- This OCP initiates a search for a gap following a long check character. Forward motion stops when the TCU senses the gap. Busy status remains true for the duration of this command. Forward motion is not stopped if end-of-tape is reached during execution of this command.

Space Forward One File (OCP '121X). -- Execution of this instruction initiates a forward search for a file mark (a 17_8 one-character record). Forward motion continues until the TCU detects a file mark and sets the end-of-file status. End-of-tape does not automatically stop forward motion.

Set Up DMC/DMA in Auto Switch Mode (OCP '131X). -- This OCP initializes the DMC/DMA subchannel in the auto-switch mode, if the TCU is so equipped, and resets the end of transmission interrupt control. Auto switch can be reset by OCP '031X or '071X.

Rewind (OCP '141X). -- This OCP initiates a rewind command to the selected transport. Up to four transports may be rewound simultaneously by executing successive rewind OCP's separated by 100 ms. The rewind OCP holds the busy status for the 100 ms duration of the rewind command.

Backspace One Record (OCP '151X). -- Execution of this OCP initiates a reverse search for a record gap. Reverse motion stops when the TCU detects a record gap. This triggers a positioning delay that stops reverse motion.

Backspace One File (OCP '161X). -- This instruction sets up a reverse search for a file mark. When a file mark is detected, a positioning delay is triggered and reverse motion is stopped.

Stop Write (OCP '171X). -- This instruction inhibits channel ready from causing an interference after the last word to be written on tape has been transferred to the TCU. This allows the end-of-motion interrupt to be independent of the channel-ready interrupt. The OCP should be issued in response to the ready interrupt for the last word in a write operation when outputting data under interrupt control.

Skip if Ready (SKS '001X). -- The ready sense line is used to test the status of the word-forming buffer. The ready line will be true when the buffer is ready for a data transfer in either direction. Data is required at the word-forming buffer at certain intervals, depending on transport speed and recording density, to sustain contiguous transfer cycles. Refer to the tables under the heading "Program Timing Considerations" for required aperture timing.

Skip if Not Busy (SKS '011X). -- The TCU will be busy upon execution of any motion command and remain busy until the motion has stopped. The TCU will also be busy for 100 ms following the execution of a rewind command or if a transport is selected and is not ready (i.e., power off, a fault has occurred, etc.).

Skip if an Error has not been Detected (SKS '021X). -- The error conditions that are checked in the TCU during the operations indicated in parenthesis (read, write, or both) are as follows.

a. Transverse parity (R/W)

b. Longitudinal parity (R/W)

c. False gap (R/W) indicates that an entire frame (character) was not read (will truncate data transfers to the computer in input mode).

d. Write echo (W) is an indication from the MTT that no heads switched for a particular frame.

e. Trespass violation (W) is an indication of excessive interchannel time displacement (frame skew).

f. Program timing error (R) indicates that the program failed to acknowledge an input data request in the specified time.

g. Low not High Error (W) is an indication from the MTT that a read signal passed the low threshold but not the high threshold.

The error sense line should be tested during a read or write operation after busy status has been reset. The error status is reset when the next TCU OCP, other than 031X, 071X, 131X, or 171X, is executed.

Skip If Not At Beginning of Tape (Loadpoint) (SKS '031X). -- The loadpoint status is tested to insure that the transport has correctly positioned the tape. The loadpoint status is true for the duration that the reflective marker on the tape is on the sense point.

When a single record has been written from the beginning of the tape, the TCU generates a 30 in. gap from loadpoint, before writing the record. If the program then executes a "Backspace One Record," the tape will not return to loadpoint but will be positioned in front of the record. If this operation is followed by another "Backspace One Record," the tape will backspace and stop on the loadpoint marker. The tape being positioned on the load point marker will inhibit reverse motion.

Skip if not Interrupting (SKS '041X). -- The conditions that will cause an interrupt are as follows:

a. The mask is set, the TCU is not in DMC/DMA mode and the TCU is ready for data transfer.

b. The mask is set, and motion is complete; i.e., TCU busy changes from true to false or a transport completes a rewind operation. On multiple transport systems, when multiple transports are rewinding, the last transport to complete rewind will cause a standard interrupt.

c. The mask is set, and the TCU is in DMC/DMA mode, and the TCU is in auto switch mode, and end-of-range is true.

The interrupt in condition a will be acknowledged by performing an INA or OTA, or by issuing OCP '171X. The interrupts in conditions b and c will be acknowledged by issuing any OCP to the TCU.

Skip if End-Of-Tape Has Not Been Detected (SKS '051X). -- The end of tape sense line indicates that a maximum of 10 ft. of tape remains usable on the reel. End of tape status will remain true until a selected transport is rewound to loadpoint, a forward or reverse command is addressed to any transport, or the system is master cleared.

The end of tape indicator has no effect on reading or writing tape. The fact that the transport has detected the end of tape tab will not stop tape movement. If reading or writing is continued indefinitely, the tape will be completely removed from the feed reel and the transport will exit from ready status and a fault will occur.

Skip if End of File Has Not Been Detected (SKS '061X). -- The end of file sense line will be set when a file mark is detected on tape during the execution of any forward or reverse command. It will be reset upon execution of the next OCP instruction addressed to the same TCU.

Upon execution of a "forward a file" or "back a file" command, after the file mark has been detected, the tape will stop slightly beyond the file mark on tape. Had the instruction been "backspace one file" and the next program instruction "read one record," the record read will be a file mark.

If a "backspace one file" is executed and there are no file marks on tape, the tape will proceed to the loadpoint and stop.

Skip if Writing is Permitted (SKS '071X). -- Writing is permitted when the write-enable ring is installed on the transport reel, the tape status switch is in the PERMIT position, and the transport is cycled up and not rewinding. This instruction applies to a transport previously selected; therefore, a suitable method of selecting a transport to be written on should be devised (such as OCP '071X, which is a no action OCP for MTT X) before issuing the SKS. (There is no TCU provision to abort a write operation command to a transport

whose reel has no file protect ring.) If a write OCP is issued to an MTT that is not permitted to write, tape motion takes place, and the TCU remains busy until the MTT is permitted to write.

Skip if MTT Operational (SKS '111X). -- The MTT is operational when its power is on, vacuum on, tape is loaded, etc. However, while it is rewinding, it is considered not operational.

Skip if DMA/DMC Sub-Channel Is Not Currently Processing Channel No. 2 (SKS '121X). -- This instruction applies to TCUs equipped with the auto-switch capability. A channel ID flip-flop is complemented at each end-of-range during automatic subchannel switching. The normal state of the flip-flop is channel ID = 1, therefore, this SKS normally skips. It does not skip after each odd numbered end of range. It is returned to ID = 1 by OCP '071X. If the DMA/DMC subchannel is not installed or not equipped for auto switch, the instruction skips.

Skip if DMC/DMA Sub-Channel is not in Auto-Switch Mode (SKS '131X). -- An auto-switch mode flip-flop in the subchannel is set by OCP '131X and reset by OCP '031X or '071X. The instruction skips if the DMC/DMA subchannel is not installed.

Skip if Not Rewinding (SKS '141X). -- When a transport is rewinding, the rewind sense line for the transport addressed will be true and may be tested anytime. At the conclusion of the rewind cycle, the sense line will become reset and loadpoint status will be true when the transport is selected.

Input From TCU if Ready (INA '001X). -- If the buffer ready status is reset, the program will treat the INA as a no-operation. If the buffer ready status is set, this instruction transfers data to the A-register and the next instruction is skipped.

Clear A-Register and Input From TCU If Ready (INA '101X). -- This instruction is the same as INA '001X except that the A-register is cleared prior to the data transfer.

Output Data To The TCU (OTA '001X). -- This instruction implements data transfer from the A-register to the TCU. The OTA skips the following instruction when executed. Data is packed 2 or 3 characters per word, depending on the mode selected, and the most significant bit is written first. Upon execution of a write OCP, the buffer is immediately ready to accept a data transfer. If the ready status is not true, the OTA is treated as a no-operation.

Set TCU Interrupt Mask (SMK '0020). -- The A-register bit assignment for TCU No. 1 is bit 1 and for TCU No. 2 is bit 2. This instruction sets the standard interrupt mask flip-flop if the A-register bit is a ONE and resets the mask flip-flop if the bit is a ZERO.

Operational and Programming Considerations

Loading Procedure

a. Set TAPE STATUS switch on control panel to TAPE CHANGE position.

b. Mount the supply reel on the right-hand hub (the hub must be held depressed to do this) and mount the takeup reel on the left-hand hub.

c. Thread loose end of tape from supply reel between the tape roller and vacuum cleaner, across the tape brake lanes underneath the magnetic head, between the tape roller and vacuum cleaner on the left-hand side, and on to the left-hand side of the takeup reel.

d. Wind 15 or 20 turns on takeup reel.

e. Depress VACUUM ON pushbutton.

f. Turn each tape reel slightly so that the tape is drawn into the loop chambers.

g. Wait until the VACUUM ON indicator is illuminated, and then set the TAPE STATUS switch to the PERMIT or PROTECT position.

h. The tape should rewind to beginning of tape, with the BOT, VACUUM ON, POWER ON, and the PERMIT or PROTECT indicators lit, and the magnetic head in the read/write position. To activate the read/write circuits, depress the R/W ON pushbutton.

File Protect Ring. -- Before writing a tape, a plastic write-enable-ring must be inserted in the groove on the back of the tape reel. This ring should be removed to prevent accidental writing on a tape that is to be "file-protected".

Reflective Tabs. -- Two reflective tabs should be present on a tape. The first should be 15 ft from the start of the tape on the edge away from the transport to indicate a loadpoint or beginning of tape. The second tab should be 25 ft from the end of the tape on the transport side to provide a means for the TCU to sense end-of-tape.

Updating Tapes. -- Information beyond the point where a new record has been written is considered to be invalid. Therefore, proper operation is not guaranteed for any forward motion command that succeeds a write command except another write command. To update a previously recorded tape each record succeeding the one updated should be rewritten.

Inter-Record Gap Lengths. -- The normal inter-record gap is nominally 3/4 in.; the gap preceding a file mark is 3 in. to 4 in. (These values neglect "forward creep" resulting from repeated rewrites of a record.)

If a record is written after backspacing a file (or a record that was a file mark), an inter-record gap of approximately 3 in. to 4 in. will result.

Loss of Primary Power. -- If primary power is lost (or shut off) while the transport(s) are powered on with vacuum on, the transport will rewind to beginning of tape (B.O.T.) and stop.

Multiple Transport Rewind. -- The busy status will remain for 100 ms following a rewind command. Another transport may be selected for rewind after this 100 ms.

MTT Logical Address. -- If a motion OCP attempts to select a transport that is not operational, or for which the selected number has not been dialed, the TCU busy status will remain until master cleared.

Although the dial on the MTT reads from 0 to 7, only 0 to 3 are meaningful in this option.

Multiple MTT Logical Addresses. -- On a given TCU, all MTTs that have dial settings corresponding to the OCP address selection will attempt to perform the instruction. If this occurs, system performance is undefined.

Incomplete Words, 3 Characters per Word Mode. -- In input mode, an incomplete word will not be transferred to the computer; i.e., if a record containing 11 characters is read with the word-forming buffer set up to read 3 characters per word, the last two characters of the record will be lost.

Incomplete Words, 2 Characters per Word Mode. -- In 2 characters per word input mode, the last character of a record containing an odd number of characters will be transferred to the computer in bit positions 1 through 6 with all other bits zero.

Non-Stop Read and Write. -- It is possible to read or write records continuously without stopping tape motion after each record. A series of OCP's that command the same direction of tape motion will be processed without interruption of motion. In a multiple system a new transport may be selected while the previously selected transport is in the process of coming to a halt.

A transport will stop in the inter-record gap if the next OCP commands a change in direction, de-selects the transport, or occurs 5 ms or more after the end of the current operation.

TCUs Equipped with DMC/DMA Subchannels. -- Data requests will occur on a channel (1 or 2) if: DMC/DMA mode is set, ready is true, channel ID is correct, and provided that end-of-transmission has not occurred. End-of-transmission occurs when external stop

(end-of-record in input mode) is encountered, or when end-of-range occurs when the subchannel is in normal DMC/DMA mode (i.e.: not in auto-switch mode).

When operating in the DMC/DMA mode, subchannel enable OCPs (031X or 131X) must precede a read or write OCP. In normal DMC/DMA mode (not auto-switch mode), OCP 031X need not be re-issued for every record transfer (i.e.: the subchannel remains in DMC/DMA mode until OCP 071X or master clear occurs). In auto-switch mode, OCP 031X, 071X or 131X must be issued after each end-of-range to clear the end-of-range storage flip-flop for subsequent data transfers.

Program Timing Considerations

The character transfer period in microseconds is as follows:

	800 bpi	556 bpi	200 bpi
80 ips	15.6	22.5	62.5
36 ips	34.7	50	139

Data requests will occur at nominal periods of 2 or 3 times the values in the table for 2 or 3 character per word modes, respectively.

Output Mode Data Request Aperture.* -- The maximum time, in microseconds, to honor output data transfer requests is as follows.

	800 bpi	556 bpi	200 bpi
		2 Characters per Word	
80 ips	30.2	44	124
36 ips	68.4	99	277
		3 Characters per Word	
80 ips	45.8	66.5	186.5
36 ips	103.1	149.0	416.0

Failure to maintain this timing will result in one of two situations:

a. If the request is not honored for 6 character periods, the record on tape will be truncated without an error indication.

b. If the request is honored after the time given above but before 6 character periods, the record will be written with one or more missing characters and an error indication will result.

Input Mode Data Availability Aperture.* -- The maximum time in microseconds to honor input data transfer requests is as follows:

---

* These aperture times are limiting values of T_{wc} in the discussion of DMC timing in Section IV of this manual.

	800 bpi	556 bpi	200 bpi
		2 Characters per Word	
80 ips	23.4	37.2	117.2
36 ips	52.6	83.2	261.2
		3 Characters per Word	
80 ips	39	59.7	179.7
36 ips	87.3	133.2	400.2

Failure to maintain this timing will result in an error indication and loss of one or more words of information.

Record Processing Times. -- Where T-start is the period between the time of a "write one record" OCP and the time that writing begins, and T-stop is the time from when the last word to be written is received from the central processor to the time when the next OCP may be issued.

	T-start	T-stop
80 ips	6.1 ms	3.5 ms
36 ips	13.6 ms	7.7 ms

Times are similar for "read one record" OCPs but can vary a great deal because of tape positioning, file gaps, and the like.

Operator Controls and Indicators

The operator control panel is centrally located above the tape deck and contains the following controls and indicators.

Control/Indicator	Function
POWER	
MAIN ON Pushbutton switch/lamp	Applies primary ac power and indicates that power is available to components and supplies.
R/W ON lamp	Indicates status of power for read/write electronics.
VACUUM ON momentary pushbutton switch and lamp	Applies ac power to vacuum pump and cycle up relays. Indicates ac power interlock is complete.
VACUUM OFF momentary pushbutton switch	Removes power from vacuum pump and cycles-down the tape transport.
Tape status rotary switch	
TAPE CHANGE position	Initiates rewind and release; cycles-down tape transport.
PROTECT position	Inhibits writing on tape.
PERMIT position	Allows writing on tape providing write-enable ring is installed on reel.

Control Indicator	Function
PROTECT lamp	Indicates TAPE STATUS switch is in PROTECT position and the tape drive is cycled up and not rewinding.
PERMIT lamp	Indicates write-enable ring is on reel, TAPE STATUS switch is in PERMIT position, and tape transport is cycled up and not rewinding.
B.O.T. momentary pushbutton	Indicates high-speed rewind to beginning of tape which is recognized by sensing the loadpoint marker.
DENSITY HIGH/LOW dual pushbutton switch	Selects density: 200 or 556, 200 or 800, or 556 or 800, depending on model.
Unit Number Selector	Selects a logical address, 0 through 3 or standby, for the MTT.

Sample Program

The following subroutine is intended as an example only. When it is called, this subroutine will read and store a forty-word BCD record (2 characters per word). The tape to be read is on MTT 2 under control of TCU 1.

```
        REL
        SUBR TAPE               Subroutine name
TAPE    DAC     **              Entry point
        LDX     =-40            Set for 80 character transfer
        SKS     '1111           Test MTT operational
        JMP     *-1             Delay until operational
        SKS     '111            Test TCU busy
        JMP     *-1             Delay until not busy
        OCP     '11             Read tape (2 characters per word)
READ    INA     '1011           Clear A and input word
        JMP     *-1             Delay if not ready
        STA     BUF+40,1        Store word
        IRS     0               Increment index
        JMP     READ            Loop to read next word
        JMP*    TAPE            Return
BUF     BSS     40              Record storage (40 words)
        END
```

FIXED HEAD DISC FILE, MODEL 516-4400

The fixed head disc file option provides an on-line bulk storage capability ranging from 98K 16-bit words to a maximum of 786K words in increments of 98K. The use of two devices with the basic disc controller gives a total storage capacity of over 1.5 million 16-bit words. Data transfers between the CPU and device can be made via the computer I/O bus alone, or via the I/O bus in conjunction with a DMC subchannel, or via a DMA bus.

Word Capacity

Track Capacity Available for Storage	1, 536 words (16-bit)
Surface Capacity Available for Storage (64 tracks/surface)	98, 304 words (16-bit)
Maximum Capacity Available for Storage	
1 Device 4 disc/8 surfaces	786, 432 words (16-bit)
2 Devices 8 disc/16 surfaces	1, 572, 864 words (16-bit)

Performance Specifications for Disc Unit

The discs revolve at a nominal speed of 3, 450 rpm. The nominal bit service rate is 1.416 kHz. The nominal word rate is 88.5 kHz. The average latency time (the time to access a location after the address has been presented to the device) is 8.5 ms with the worst case condition a maximum of 17.5 ms. The nominal bit period is 0.706 μsec.

The option operates on-line in both the read and write modes. Provisions are made for variable sector (record) length operation.

Character Addressing Format. -- Data is organized bit serially in 64 concentric tracks on each surface. Each track is logically divided into 8-bit character segments. The controller allows a position on a track to be accessed by a corresponding character address. Each of the 3072 functional character addresses within a track designate a possible starting position for data transmission. Integral numbers of character segments are grouped to form records or sectors.

Serial Data Format. -- Data is organized on the disc so that bit 1 of the computer word is the first bit and bit 16 is the last bit transferred to (from) the control segment.

Gap Format. -- The gap character formed at the end of each record is a full character segment, the first bit of which represents the even parity of its associated record. The remaining seven bits are undefined.

Write Mode. -- A written record begins at the character addressed and spans contiguous character segments (two per output word transfer) for a period (measured in integral characters) equal to the number of sustained output word transfers from the computer.

A failure to meet the output word transfer rate requirement of the disc will cause the controller to form a gap character and terminate the write.

Sustained output data transfers of varying lengths will result in writing records of correspondingly varying lengths each followed by a gap character. There are no limitations on the variation of record size within a track or between two tracks other than those imposed by the requirement for unambiguous use of the available character segments. A record may not exceed the track capacity. Data transmission is automatically terminated upon detection of the track origin.

Read Mode. -- Data transmission to the computer, in the input mode, begins at the addressed character and spans contiguous character segments for a period equal to the number of sustained input data transfers. A failure to meet the input word transfer rate requirement of the disc will cause the controller to interpret the character following the last data character as the gap character and terminate the read.

Sustained input data transfers of varying lengths not corresponding to the written data will result in incomplete or invalid data and invalid parity. Similarly input transfers that originate at the character address other than the starting character address of the corresponding written data will result in partial or invalid data and incorrect parity. Data transmission is terminated upon detection of the track origin.

Programming

The address for this option is 22. The instruction assignments are as follows:

SMK '0020 sets the interrupt mask for the Disc Channel if the corresponding A-register bit 8 equals "one" and resets the interrupt mask if the corresponding A-register bit 8 equals "zero."

INA '0022	Input from the Disc File if ready
INA '1022	Clear A and input from the Disc File if ready
OTA '0022	Output to the Disc File if ready
OCP '0322	Select DMA or DMC operation
OCP '0422	Stop data transfer/acknowledge interrupt
OCP '0722	Select I/O bus operation
SKS '0022	Skip if Fixed Head Disc File ready
SKS '0122	Skip if Fixed Head Disc File is not busy
SKS '0222	Skip if Fixed Head Disc File has not detected a data transfer error
SKS '0322	Skip if Fixed Head Disc File has not detected an access error
SKS '0422	Skip if Fixed Head Disc File is not interrupting.

Input from Disc File if Ready (INA '0022). -- If the buffer ready status flip-flop is not set, the program will execute the instruction following the INA. When the buffer ready is true, the instruction will transfer the data to the A-register, and the next sequential instruction will be skipped.

Clear A and Input from Disc File if Ready (INA '1022). -- This instruction is identical to INA '0022 except that the A-register is cleared before the data is transferred.

Output to Disc File if Ready (OTA '0022). -- This instruction implements data transfer from the A-register to the disc file. The OTA skips when executed. Data is packed eight-bits-per-character, two characters/word, with the most significant bit written first.

Select DMC or DMA Operation (OCP '0322). -- This OCP must be issued to initiate a record transfer via DMC or DMA. It conditions the channel to initiate setup words and data transfer.

Stop Data Transfer/Acknowledge Interrupt (OCP '0422). -- This OCP has two functions:

a. Stop Data Transfer -- Must be issued when operating in I/O bus mode to terminate a record transfer. It must be issued within 11 μs of the "READY" for the last word. When operating in DMC/DMA mode, this function is performed by ERL.

b. Acknowledge Interrupt -- The standard interrupt (PIL) will occur from a transition to "Not Busy" until the next select OCP is issued providing this option is masked on. The interrupt line (PIL) may be returned to its quiescent state, however by issuing OCP '0422. This function of the OCP will normally be used only when operating in DMC/DMA mode.

Select I/O Bus Operation (OCP '0722). -- This OCP must be issued to initiate a record transfer via the standard I/O bus. It conditions the channel to initiate setup words and data transfer.

Skip if Fixed Head Disc File Ready (SKS '0022). -- Execution of this instruction will cause the program counter to skip if the channel is ready to accept a word transfer.

Skip if Fixed Head Disc File is Not Busy (SKS '0122). -- Busy becomes true upon receipt of OCP '0322 or '0722 and remains true for the duration of an address search and consequent data transmission. In the read mode, busy is reset one or two character times (5.5 or 11 μs) following the last computer input transfer. In output mode busy is normally (record contains more than three words) reset five or six character times (28.0 or 33.6 μs) following the last computer output transfer (if one or two words, latency period occurs after last computer transfer. It is also reset by an access error (see SKS '0322).

Skip if Fixed Head Disc File has not Detected a Data Transfer Error (SKS '0222). -- Execution of this instruction will cause the program to skip if a Data Transfer error has not been detected. This status line will indicate one of two errors, either of which is probably recoverable: a) Parity Error -- Parity checking is performed on a record basis in read mode only. There is one parity bit (even parity) per record; and it occupies the first bit position of the character following the last data character. b) Timing Error -- If OCP '0422 (stop Data Transfer in I/O mode) or ERL occurs after the disc has lost SYNC, this status line indicates that ready honoring intervals have not been sustained or a track origin has been encountered during a record transfer.

This status line is reset by either select OCP ('0322 or '0722) or master clear.

Skip if Fixed Head Disc File has not Detected an Access Error (SKS '0322). -- An access error will result from one of the following conditions:

a. Selecting a non-existent device (Disc File).

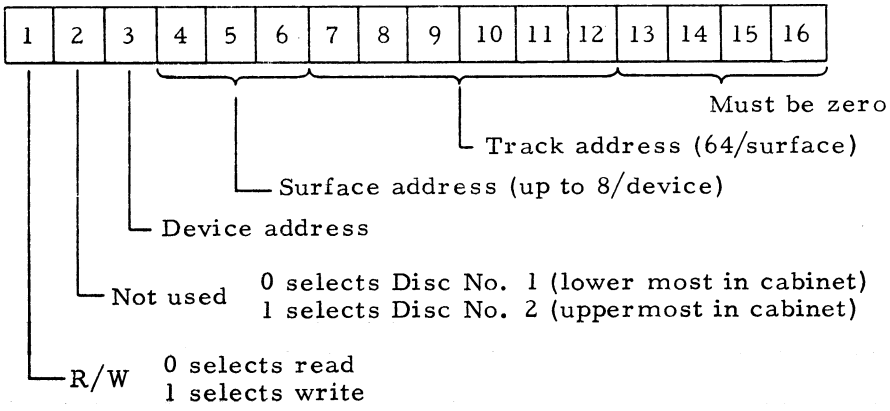
b. An attempt to write on a write-disabled device. (See write lockout switches.)

c. Selecting a non-existent character address. This error resets busy and persists for duration of error condition.

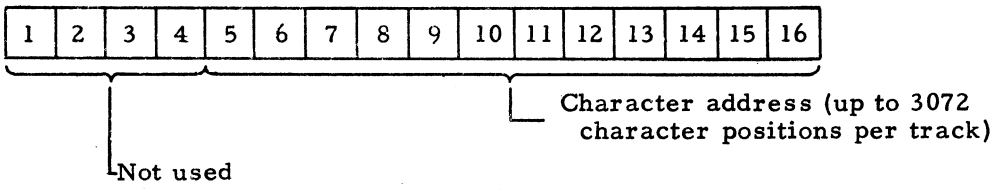
Skip if Fixed Head Disc File is Not Interrupting (SKS '0422). -- Execution of this instruction will cause the program to skip if the channel is not interrupting (see OCP '0422 Section II for description of interrupt).

Set-up Sequencing. -- Both read and write modes share a common set-up sequence, consisting of an OCP and two OTA instructions. The OTAs function to transmit from the computer to the controller the addressing information necessary to transfer data to (from) a distinct starting position on the disc.

First Word



Second Word



I/O Bus Operation

OCP '0722

Two OTAs

Wait for Ready

DMA Operation

DMA setup

OCP '0322 (See Section IV.)

NOTE

The two setup words will occupy the first two words in the data block and will be transmitted to the channel via DMA bus in Output mode. After the first two transfers, the disc file will condition the DMA control logic for the appropriate mode, input or output.

DMC Operation

DMC setup (See Section IV)

OCP '0322

Two OTAs

NOTE

The two set-up words will be transmitted to the disc file with OTAs. After that data transfer will automatically proceed in DMC mode.

Access Timing Considerations.

A Disc Setup Timing

In the output mode, the controller will begin a search for the starting character position following the setup instruction sequence and the first data output transfer. Data communication with the device is inhibited for the duration of 70 bit times (50 μs) following the start of a search operation.

In input mode, the controller will begin a search for the starting position 7 to 14 bit times (4.9 to 9.8 μs) after the setup words are transferred to the channel. Data communication is inhibited for 70 bit times (50 μs) after the beginning of a search operation.

Failure to stay within these timing considerations will extend the search operation time by one revolution (17 milliseconds).

Input/Output Timing

During continuous transmission on the I/O bus or the DMA, a true channel ready status must be honored within 11 μs. When operating with the DMC a service request must gain response within 18 μs. Failure to comply with these timing requirements will result in termination of data transmission.

a. Track to Track Accessing

A data transfer overlapping two tracks requires a separate setup for each track. Use of a full data complement on the first track will result in an additional one revolution delay for the second track access. To avoid this delay in data transmission, time must be provided to allow the completion of the next setup before the addressed character position of the second track is reached. There are 48 bit times (33.6 μs) available between the end of the last word on a track and the track origin.

In addition, 8 bit times are available between track origin and the first character position. These 56 bit times are available as part of the total time required to make a head address change (70 bit times).

b. Disc to Disc Accessing

In a configuration containing two devices, track origin clocks are asynchronous. If a device select change is specified in the setup word, the controller must be synchronized to the new track origin. Therefore, the access time will be up to a full revolution plus the latency period of the addressed position.

Controls and Indicators

Controls and indicators on the control panel (Figure 5-5) and on the disc unit indicator panel (Figure 5-6) are described in Table 5-5 and in Table 5-6, respectively.

Write Lockout Switches. -- In addition to the Write Disable switches (located on the Mass Memory Control panel) each unit is supplied with 16 separate Write Lockout switches which control the write function of the first 128 read/write heads (tracks 0 through 127). Each lockout switch controls a group of 8 tracks as follows:

Switch 1 controls tracks 0 through 7

Switch 2 controls tracks 8 through 15

↓

Switch 16 controls tracks 120 through 127

Any combination of the above switches may be used.

NOTE

The program receives no indication of the status of the lockout switches; the only visual indication of their status is the position of the switches themselves.

Table 5-5.
Control Panel, Controls and Indicators

Control or Indicator	Function
OFF LINE POWER switch	Three-position toggle switch
ON LINE (center)	Allows ac power to be distributed in device cabinet under control of computer.
OFF (down)	Removes ac power from device cabinet; independent of computer power status.
ON (up)	Applies power to device cabinet; independent of computer power status. Also puts controller into off-line read mode.
WRITE DISABLE switch	Two-position illuminated toggle switch which allows the following three operations:
BOTH (center)	Disables write operation on both upper and lower disc units.
LOWER (down)	Inhibits write operations on lower disc unit and permits write operations on upper disc unit.
UPPER (up)	Inhibits write operations on upper disc unit and permits write operations on lower disc unit.
AC POWER indicator	Indicates ac power status in device cabinet
10 AMP fuse	Over-current protection for ac power distribution in device cabinet.

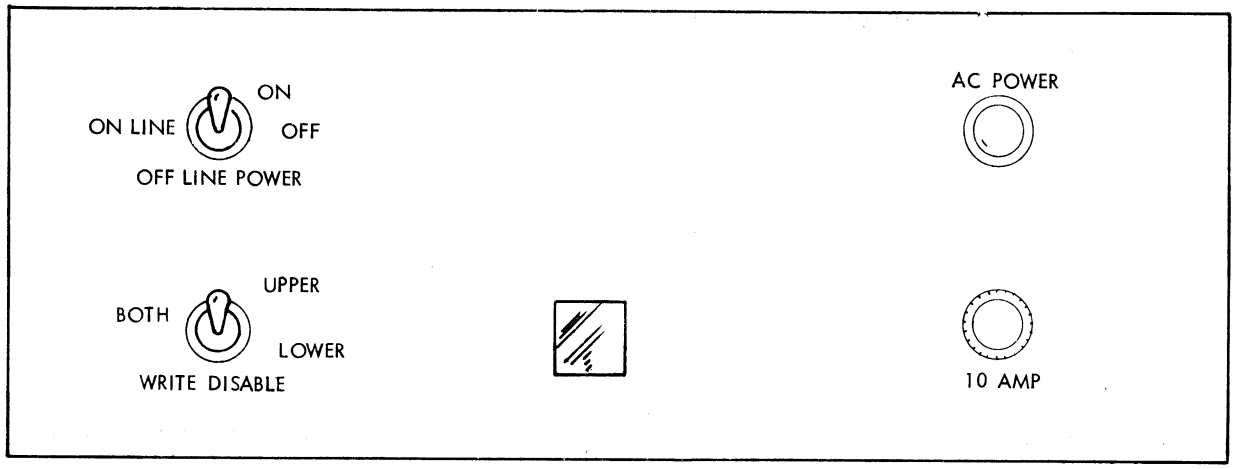


Figure 5-5. Control Panel, Controls and Indicators

Table 5-6.
Indicator Panel, Controls and Indicators

Control or Indicator	Function
ACTUATION PRESSURE LOW indicator	Illuminated when power is applied to an internal pump in device which maintains correct head plate actuation pressure.
DRUM SPEED LOW indicator	Illuminated when disc speed is less than 3100 rpm (approximate).
TEMP HIGH indicator	Illuminated when device shroud temperature exceeds 150°F or if motor winding temperature exceeds 300°F.
MOTOR RESET pushbutton switch	Reapplies, when depressed and released, line voltage to device drive motor, pump, and solenoid pump valve following overtemperature condition.
MOTOR POWER ON indicator	Illuminated when 115 Vac power cable connected and active.

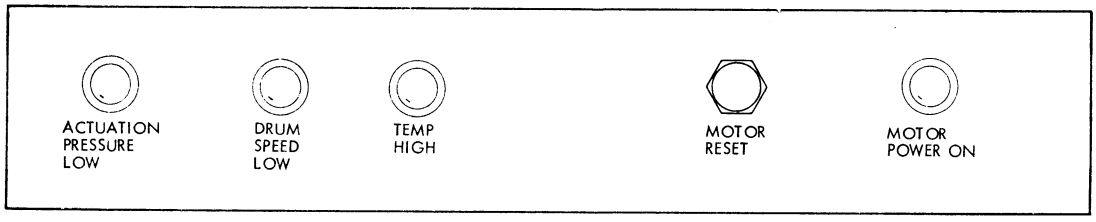


Figure 5-6. Disc Unit Indicator Panel, Controls and Indicators

MOVING HEAD DISC FILE, MODEL 516-4600

General Description

This option consists of a Disc Control Unit (DCU) capable of controlling up to four Disc Storage Drives. The drives may be either Model 4621 (200 track/surface device) or Model 4260 (100 track/surface device).

The recording medium is the IBM 1316 Disc Pack. This is an assembly of ten magnetic oxide coated disc surfaces on a common shaft. It comes with a plastic handle and cover assembly. The handle and cover assembly is used to remove the disc pack from the drive and to protect the disc during storage.

Storage Capacities. (See also Figure 5-7)

The following table shows the maximum number of 16-bit words based on one record-per-track, and in parenthesis the number of 16 bit words based on 1-word records (103 records-per track):

	4621		4620	
Words per track	1,800	(103)	1,800	(103)
Words per surface	360,000	(20,600)	180,000	(10,300)
Words per device	3,600,000	(206,000)	1,800,000	(103,000)
Words per option	14,400,000	(824,000)	7,200,000	(412,000)

Access Time

For approximate access time see Figure 5-8.

Record Format

The record format is shown in Figure 5-9. All fields, A through L, are written during a track format. Field A is written once at the beginning of the track. Field B through L are formatted for each record. Field G (data field) may be pseudo data or actual data during track format. Field L is 5% of the number of bits in the record (fields B through K).

A write one record instruction does not alter fields A through D. It does rewrite fields E through K. It does not rewrite the 5% gap. During this instruction field G (data) may contain from 1 to 1800 words. If compatibility with the DDP-124 Moving Head Disc option is desired the data must be in multiples of three words.

A read one record instruction does not alter any fields.

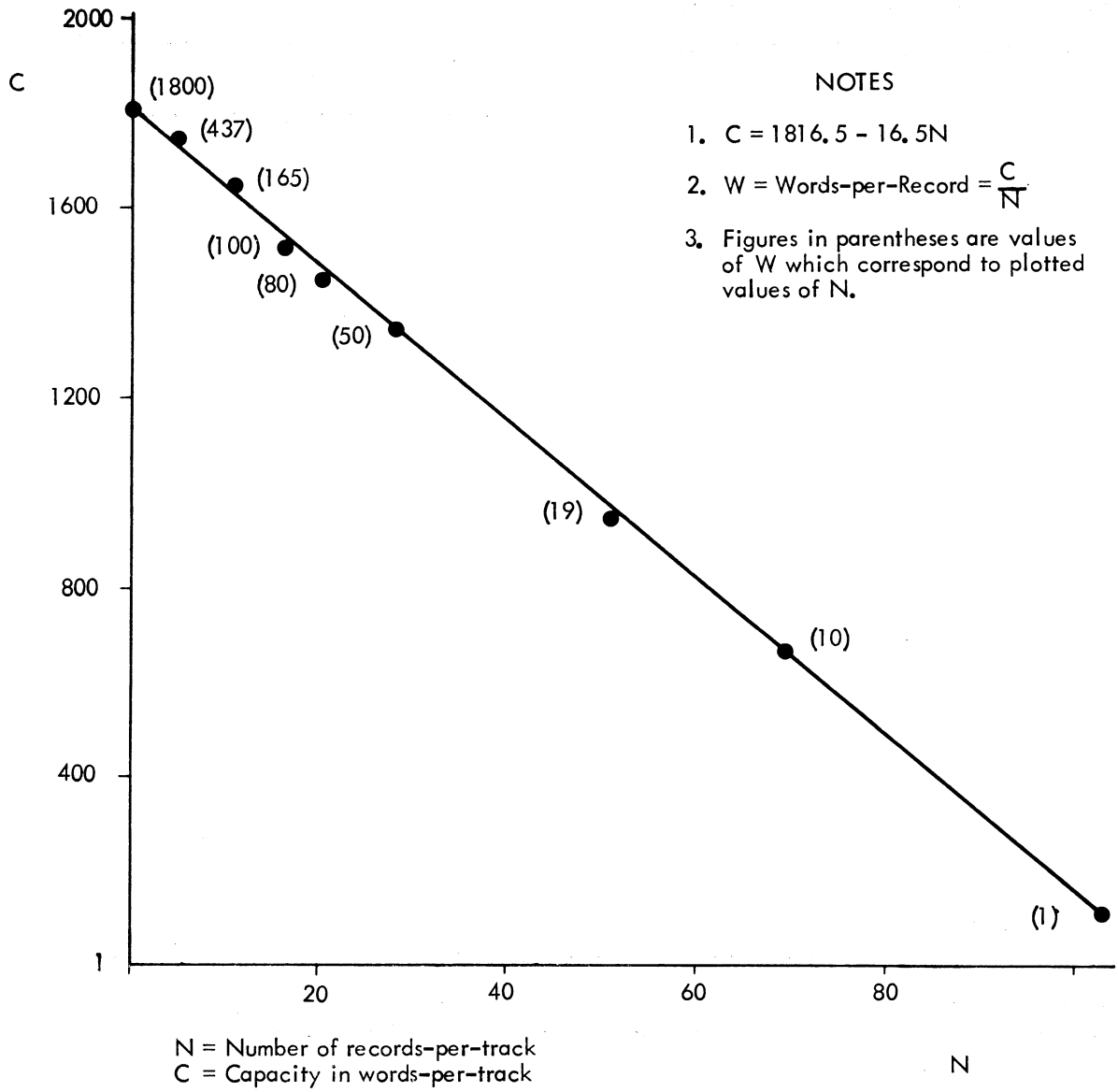


Figure 5-7. Track Capacity as a Function of the Number of Records Per Track

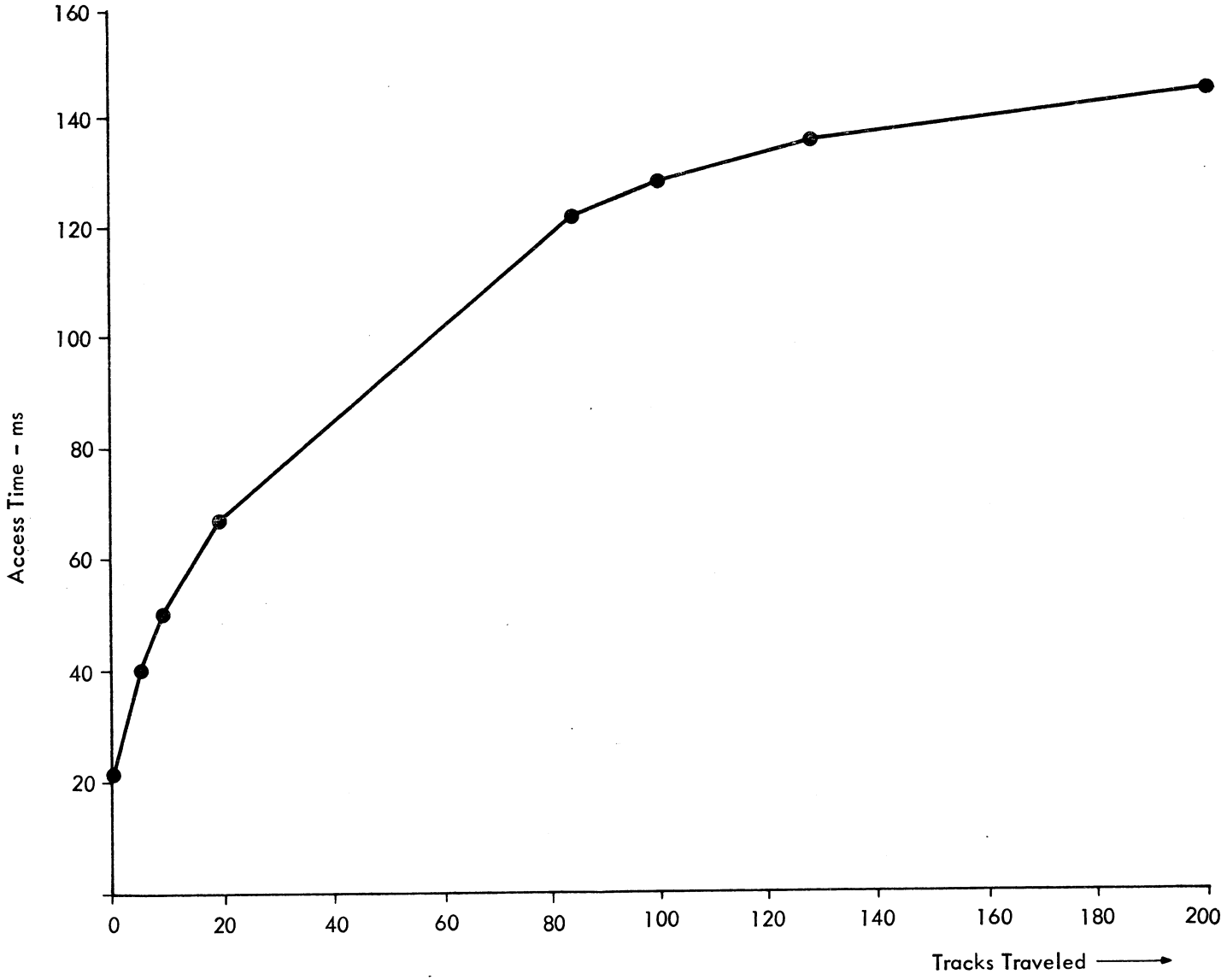


Figure 5-8. Approximate Track Positioning Times

Programming Instruction Assignments

The address for this option is 25; and the mask bit assignment for use with SMK'0020 is bit 4. Instructions are as follows:

INA '1025	Clear A and input from disc file if ready.
INA '0025	Input from disc file if ready.
OTA'0025	Output to disc file if ready.
OCP'0025	Return to zero seek
OCP'0125	Direct seek
OCP'0225	Read current address
OCP'0325	Enable DMC/DMA mode of data transfer
OCP'0525	Write track format
OCP'0625	Read/write record
OCP'0725	Enable I/O bus mode of data transfer
OCP'1025	Stop transfer
OCP'1425	Acknowledge interrupt
SKS'0025	Skip if ready
SKS'0125	Skip if not busy
SKS'0225	Skip if no data error
SKS'0325	Skip if no set up error
SKS'0425	Skip if not interrupting
SKS'1425	Skip if Unit No. 1 not seeking
SKS'1525	Skip if Unit No. 2 not seeking
SKS'1625	Skip if Unit No. 3 not seeking
SKS'1725	Skip if Unit No. 4 not seeking

Input from Disc File if Ready (OTA '0025). -- This instruction is identical to INA '1025 except the A register is not cleared.

Clear A and Input from Disc File if Ready (INA '1025). -- If ready is true this instruction clears the A register, transfers a word from the Disc Control Unit (DCU) channel register to the A register via the input bus, and causes the next instruction to be skipped.

If ready is false the instruction is treated as a no-op.

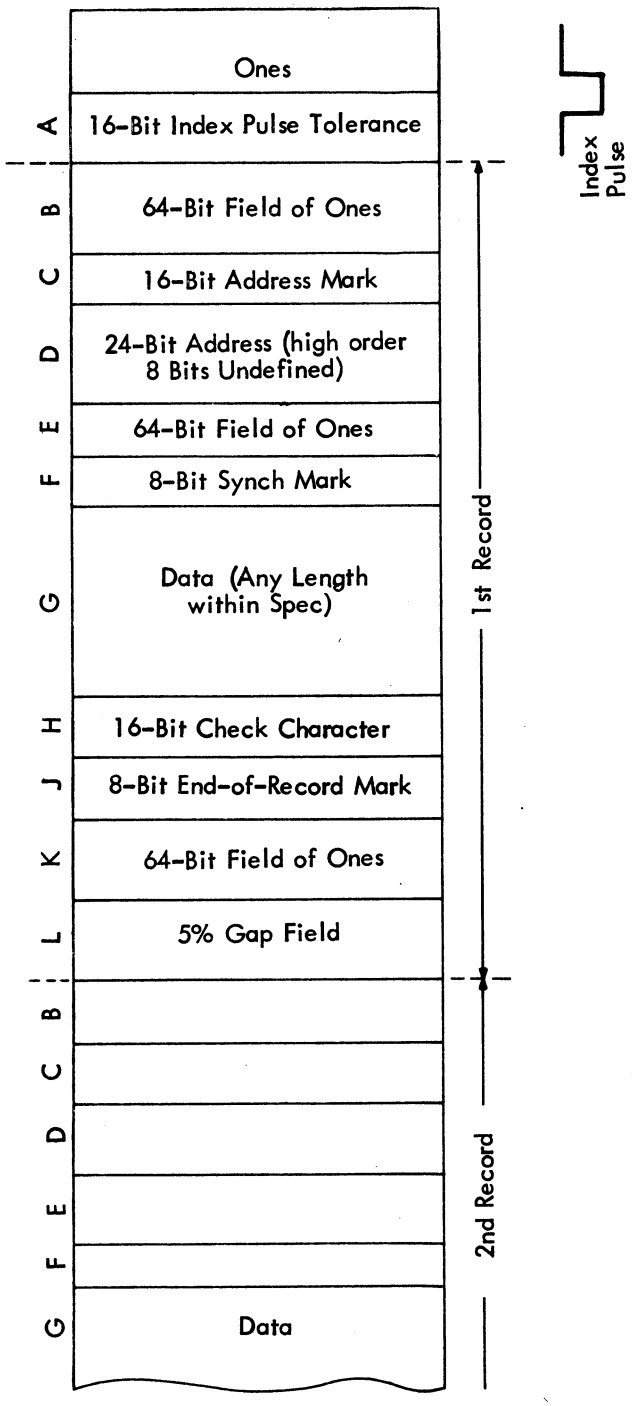


Figure 5-9. Record Format

Output to Disc File if Ready (OTA '0025). -- If ready is true this instruction transfers a word from the A register to the DCU channel register via the output bus and causes the next instruction to be skipped.

If ready is false this instruction is treated as a no-op.

OCP Instructions. -- All OCPs except '1025 and '1425 are ignored by the DCU if issued when the DCU is busy. OCPs '0025, '0125, '0225, '0525, and "0625 all require set up information (see Figure 5-10) via I/O bus or DMA bus to complete the desired operation (details to follow in OCP descriptions).

Return to zero seek (OCP '0025). -- This OCP, with its associated setup word, moves the heads on unit No. 1 (i = 0, 1, 2, or 3 for the four possible devices) to track 000. The DCU is busy for 50 μs starting with the setup word OTA; and unit No. i will be seeking for 70 to 500 ms after the OTA. Simultaneous head motion on multiple unit DCUs may be accomplished by successive OCPs and OTAs providing DCU busy (SKS '0125) is honored between each OCP.

Direct Seek (OCP '0125). -- This OCP, with its associated setup word, moves the heads on unit No. i the number of tracks specified by bits 9 through 16 of the setup word in the direction specified by bit 8 of the setup word. Direction is defined as follows: if bit 8= 1 the heads move toward the outside of the disc (reverse); if bit 8=0 the heads move toward the center of the disc (forward). A seek of zero tracks would hang up a disc storage drive; therefore the DCU will detect difference = zero and treat as a no-op, and generate an interrupt The DCU is busy for 50 μs after the OTA; and unit No. i is seeking for 30 to 165 ms after the OT OTA. Simultaneous head motion on multiple unit DCUs may be accomplished by successive OCPs and OTAs providing DCU busy is honored between each OCP. (See seek Operations for Programming.)

Read Current Address (OCP '0225). -- This OCP, with its associated setup word, reads the address of the most current record at the time of the OTA on unit No. i and head No. j (j=0 through 9). Upon receipt of the setup word the DCU searches for an address mark (field C) and makes the associated address (field D) available on the input bus. The DCU is busy from the set-up OTA to the time when the address is available to the central processor. The DCU becomes not busy (with resultant interrupt) when ready is set. (See Table 5-7.)

Note: The actual address on the disc consists of 24 bits of which 8 are undefined. The 516 option will format a 24 bit address, but only 16 bits will be under control of the program (only 16 bits transferred from DCU to central processor).

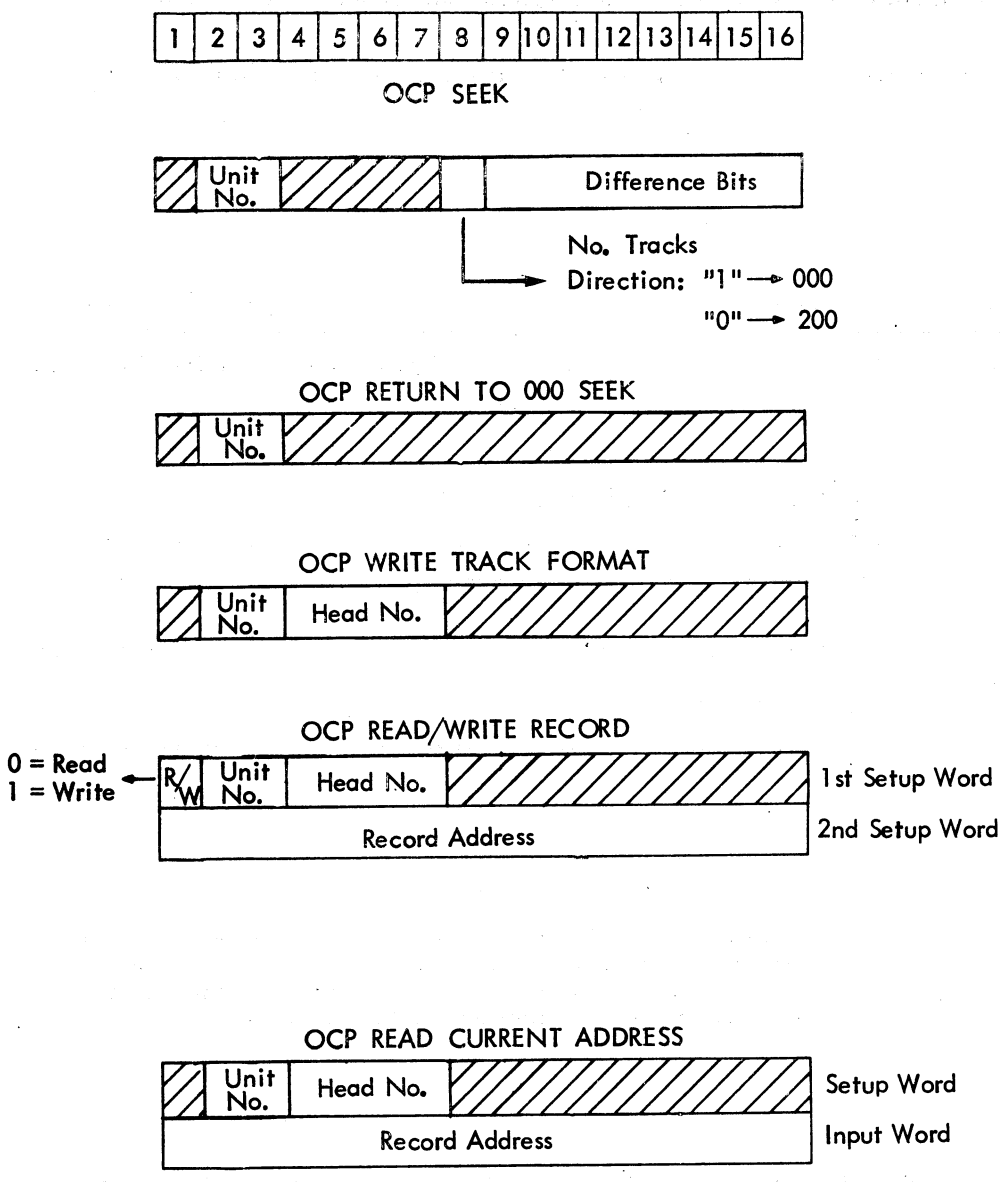


Figure 5-10. Set-Up Word Formats

Enable DMC/DMA Mode of Data Transfer (OCP '0325). -- This OCP enables the DCU to transfer data utilizing the DMC or DMA if equipped with the appropriate sub-channel. It does not initiate any read, write, or motion commands. Depression of the master clear button initializes the DCU in DMC/DMA mode. The DCU will remain in the DMC/DMA mode until OCP '0725 is issued. When this OCP instruction is required, it should precede a read or write OCP.

Table 5-7.
Read Current Address

Step	I/O Bus	DMC	DMA
1		Initialize DMC (input), range = 1 word = address to be read	Initialize DMA (output), range = 2 First word = setup Second word = address to be read
2	OCP '0725	OCP '0325	OCP '0375
3	OCP '0225	OCP '0225	OCP '0225
4	OTA set up word	OTA set up word	(enter DMA)
5	INA current address after set up OTA (see note a)	(enter DMC)	(DCU switches DMA control to input)
6	OCP '1025 not required	(end-of-range)	(end-of-range)

NOTE

Timing of the INA is not critical. The Read Current Address operation may be treated as an "off line" function since the NOT BUSY interrupt at the end of the operation is coincident with data ready.

Write Track Format (OCP '0525). -- This OCP, with its associated setup word, writes an entire track of records on unit No. i and head No. j. It does not initiate any head motion. It is used to write a track for the first time or to change the format of records on a track. DCU busy is true from the setup word OTA until the format operation is terminated at track origin. (See Table 5-8.)

The 5% gap (field L) is formed under programming specified in Table 5-8. The value of the 5% gap word is 5% of the number of bits in the record including 264 bits (16.5 words) of overhead.

To guarantee access to sequential records on a track for subsequent read or write operations the following two conditions must be met:

a. The 5% gap word must be increased by Δ bits

Δ bits = 28 bits + (1.25 bits/μs) (T μs)

where T is the program time between busy going false (end of a read or write operation) and receipt by the DCU of the first setup word for the next read or write operation (OCP '0625 sets ready for this setup word).

b. The ready for the second setup word (address of new record) must be acknowledged in no more than 28 μs. This second ready becomes true 50 μs after the DCU receives the 1st setup word.

If the output transfer rate is not maintained by the computer the DCU will abort the format operation, write gap to track origin, and set the data error sense line.

Table 5-8.
Write Track Format

Step	I/O Bus	DMC	DMA
1		Initialize DMC (output), range = n + 1 First word = address n = No. of data words	Initialize DMA (output), range = n + 2 First word = setup second word = address n = No. of data words
2	OCP '0725	OCP '0325	OCP '0325
3	OCP '0525	OCP '0525	OCP '0525
4	OTA setup word	OTA setup word	(enter DMA)
5	OTA first record address word within 64 μs	(enter DMC)	
6	OTA first data word within 57 μs		
7	OTA subsequent data words within 12 μs		
8	OCP '1025 within 12 μs of last data word	(end-of-range)	(end-of-range)
9		Reinitialize DMC/DMA for range = n + 2 within 50 μs of end-of-range. First word = 5% gap for previous record Second word = current record address n = No. of data words	
10	OTA 5% gap word within 64 μs of OCP '1025	(enter DMC)	(enter DMA)
11	OTA next record address within 50 μs of 5% gap word, etc. (i.e. repeat steps 5 through 10 for each record		
12	OCP '1025 after last 5% gap word to stop	Initialize DMC/DMA for range = 1 for last 5% gap word	

NOTE

Disc writes gap through to 64 bits beyond index, therefore, cylinder mode formatting requires 2 revolutions for each track.

Read/Write Record (OCP '0625). -- This OCP, with its two associated setup words, will read or write (bit 1 of first setup word) one record on unit No. i and head No. j (specified by first setup word) at the record address specified by the second setup word. It does not initiate any head motion. (see Tables 5-9 and 5-10.)

READ OPERATION (Bit 1 of first setup word = 0).

Data in the addressed record will be read until one of the following conditions occurs:

a. The index pulse is encountered while reading.
b. Input transfer rate is not maintained the by computer.
c. End-of-record is sensed.
d. Stop transfer OCP is issued or DMC/DMA end-of-range occurs. Data transfer will cease, but the DCU will continue reading to end of record.

DCU busy will be true from the first setup word OTA until one of above conditions a through c occur.

If the range specified by the program (number of words to be read) is larger than the number of words in the record, the check word (field H) will be transferred to the central processor.

WRITE OPERATION (Bit 1 of first setup word = 1).

Data will be written (number of words to be $\leq$ number of words determined by the format) continuously at the addressed record until one of the following conditions occurs:

a. The index pulse is encountered while writing.
b. Output transfer rate is not maintained by the computer.
c. Stop transfer OCP is issued or DMC/DMA end-of-range occurs.

Except for condition a, the word being written will be completely written; and the write instruction will be terminated by writing a check character, end of record, and field of ones (fields H, J, and K of Figure 5-7). DCU busy will be true from the first setup word OTA until one of the above three conditions occurs.

If new data (field G^1) is greater than that determined by the format (field G), the following conditions exist:

a. If G^1 G + 4 words a corresponding reduction in field L (gap) will occur, but the next record will not be affected.

b. If $G^1 > G + 4$ words the next record may be destroyed, but records following will be unaffected unless the amount by which $G^1 > G + 4$ is more than a record.

Table 5-9.
Write One Record

Step	I/O Bus	DMC	DMA
1		Initialize DMC (output), range = n (n = No. of data words)	Initialize DMA (output), range = n + 2 First word = Setup No. 1. Second word = Setup No. 2. n = No. of data words
2	OCP '0725	OCP '0325	OCP '0325
3	OCP '0625	OCP '0625	OCP '0625
4	OTA set up No. 1	OTA set up No. 1	(enter DMA)
5	OTA set up No. 2 (see Note a)	OTA set up No. 2	
6	OTA first data word within 83 μs of set-up No. 2	(enter DMC)	
7	OTA subsequent data words within 12 μs		
8	OCP '1025 within 12 μs of last data word	(end-of-range)	(end-of-range)

NOTE

Timing for sequential record access is specified under Write Track Format (OCP '0525). If sequential access is not desired, timing of second setup OTA is not critical.

Table 5-10.
Read One Record

Step	I/O Bus	DMC	DMA
1		Initialize DMC (input), range = n (n = No. of data words)	Initialize DMA (output), range = n + 2 First word = Setup No. 1 Second word = Setup No. 2 n = No. of data words
2	OCP '0725	OCP '0325	OCP '0325
3	OCP '0625	OCP '0625	OCP '0625
4	OTA setup No. 1	OTA setup No. 1	(enter DMA)
5	OTA setup No. 2 (see Table 5-9 Note)	OTA setup No. 2	
6	INA first data word within 96 μs of setup No. 2	(enter DMC)	(DCU switches DMA control to input after setup)
7	INA subsequent data words within 12 μs		
8	OCP '1025 within 12 μs of last word to be read	(end-of-range)	(end-of-range)

Enable I/O Bus Mode of Data Transfer (OCP '0725). -- This OCP disables DMC or DMA mode of data transfer and enables data transfer via the standard I/O bus. It does not initiate any read, write, or motion commands. The DCU will remain in I/O bus mode until receipt of OCP '0325 or the master clear button is depressed. When this OCP instruction is required it should precede a read or write OCP.

Stop Transfer (OCP '1025). -- This OCP is required in I/O bus mode to terminate a record transfer when writing a record or during write track format. Also during write track format, formatting of the track will be discontinued if this OCP is issued after the 5% gap word is received by the DCU, at which time ones are written to the track origin.

This OCP will terminate data transfer during a read instruction, and is required if the number of words to be read $\leq$ the number of words in the record to avoid an invalid indication of data error (condition 2 of SKS '0225).

Acknowledge Interrupt (OCP '1425). -- This OCP is provided to remove the interrupt which is caused by the following conditions:

a. Mask set and DCU NOT BUSY (i.e., when the DCU busy signal changes from true to false, an interrupt flip-flop is set which may be reset by this OCP or any OCP addressed to the DCU). An interrupt does not occur for the 50 μs busy condition resulting from a seek operation.°

b. Mask Set and SEEK COMPLETE.
If more than one unit is seeking, each unit to complete seeking will cause the interrupt. If DCU busy is true when seek somplete occurs, the seek complete interrupt will be held inactive till DCU busy becomes false. The DCU will cause an interrupt immediately upon receipt of a set up word which specifies a difference of zero tracks for a direct seek operation. The seek complete interrupt is acknowledged by any OCP addressed to the DCU including OCP '1425.

Skip if Ready (SKS '0025). -- This instruction skips if the DCU is ready for transfer of a word to/from the computer.

Skip if Not Busy (SKS '0125). -- This instruction skips if the DCU is not busy. DCU busy is described in the foregoing OCP descriptions.

Skip if No Data Error (SKS '0225). -- This instruction skips if no data error has occurred. The data error sense line is valid only after the DCU is not busy. Following are the data error conditions:

a. Check bit comparison failure during read.
b. Failure of computer to sustain the data transfer rate in read or write (including track format) prior to OCP '1025 or DMC/DMA end of range.

Sense line is reset by any OCP addressed to the DCU except OCP '1025 and '1425.

Skip if No Setup Error (SKS '0325). -- This instruction skips if no set up error has been detected. This sense line is valid only after the DCU is not busy, and is reset by any DCU OCP except OCP '1025 and '1425. Following are the set up error conditions:

a. Record address comparison failure.
b. An attempt to seek to a track address less than 000 or greater than 202/99 for 9433/9433A device. If this occurs, the device will perform a return to zero operation and produce a seek complete response to the DCU.
c. The selected unit is not online.
d. Index pulse is encountered while writing or reading.
e. No unit has been selected.

f. Data unsafe conditions from the disc drive:
   1. More than one head selected
   2. Both read and write gates selected
   3. Erase and no write driver selected
   4. Both write drivers on
   5. Read or write selected and not on cylinder.

Skip if Not Interrupting (SKS '0425). -- This instruction skips if the DCU is not interrupting Interrupt conditions are described under OCP '0425.

Skip if Unit No. 1 Not Seeking (SKS '1425). -- This instruction skips if Unit No. 1 is not seeking. The duration of seek is described under OCPs '0025 and '0125.

Skip if unit No. 2 not seeking (SKS '1525)
Skip if Unit No. 3 no seeking (SKS '1625)
Skip if Unit No. 4 not seeking (SKS '1725)

These are same as SKS '1425 except for unit identification.

Data Transfer Timing

During continuous transmission with I/O bus, DMC, or DMA a true channel ready status must be acknowledged within 12 μs to avoid a data error (SKS '0225 condition 2). This is the limiting value of T_{wc} in the discussion of the DMC option.

Instruction Sequences

Tables 5-7, 5-8, 5-9 and 5-10 describe proper instruction sequences for the read and write operations for a given DCU configuration (i.e., I/O bus only, DMC, or DMA).

Seek Operations

a. I/O Bus or DMC configurations require only the appropriate OCP ('0025 for return to zero, or '0125 for direct seek), followed by an OTA '0025 for the setup word.
b. DMA configurations require initialization of DMA in the output mode with range equal to one word (the setup word), followed by the appropriate OCP ('0025 or '0125).

Operator Controls and Indicators

Start. -- This switch, when depressed, will energize the spindle drive motor and begin the "first seek" sequence.

Unit Number. -- This indicator is illuminated when the heads are loaded on the pack. It indicates the number assigned to each drive (o through 3) in a multiple drive system.

Fault. -- This indicator/switch is illuminated when unwanted conditions exist that would cause loss of data (see also SKS '0325 description); and, when depressed, will clear the fault until the source of the problem reappears.

Disc Pack Installation and Removal

Installation. -- Before installing a disc pack, set the power supply MAIN POWER circuit breaker to ON. Do not press the START switch/indicator.

a. Grasp the disc pack by the cover handle and raise it from the storage surface.
b. Unscrew the bottom cover from the disc pack assembly using the knob located on the bottom of the disc pack. Set the bottom cover to one side.
c. Raise the plexiglass cover on the disc storage drive assembly (Figure 5-11).

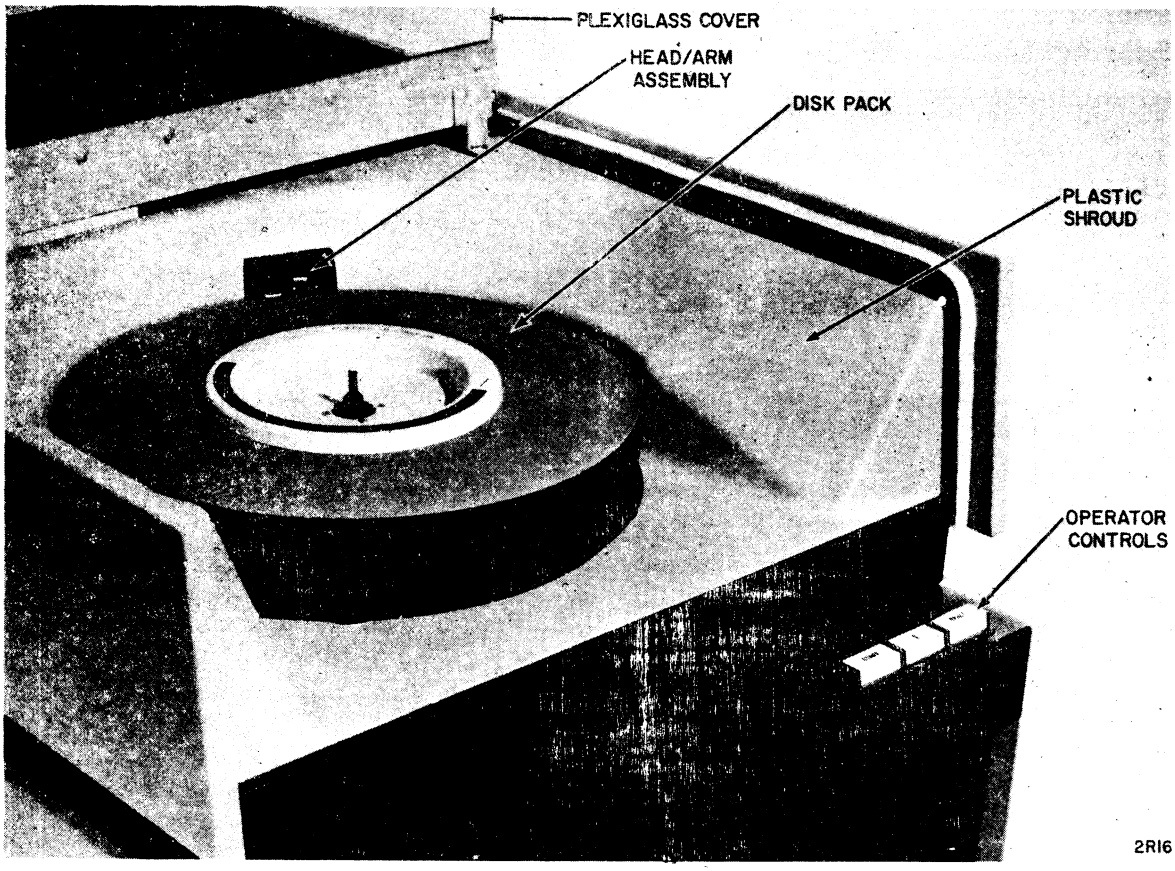


Figure 5-11. Disc Pack Load and Unload Mechanics

d. Place the female conical surface of disc pack onto the male spindle assembly. Use care to avoid bumping the disc pack against the spindle assembly. Do not touch either the spindle or the mating disc pack surface with the fingers. Corrosion will result.

e. Twist the disc pack handle clockwise until the disk pack is firmly seated on the spindle.

f. Raise the disc pack cover and remove it from the shroud area.

g. Close the plexiglas cover immediately after removing the disc pack cover. This prevents the entry of dust and the contamination of the discs.

Removal. -- Prior to removing the disc pack, make certain that the pack has stopped rotating.

a. Raise the plexiglas cover on the disc storage drive.

b. Place the disc pack cover over the mounted disc pack. Using the tips of the fingers, twist the cover until it is seated.

c. Grasp the disc pack cover handle and twist it counterclockwise until the pack is free.

d. Remove the disc pack from the shroud area.

e. Lower the plexiglas cover on the shrouded area.

f. Place the bottom cover into position on the disc pack and tighten it into position.

PROCESS INTERFACE CONTROLLER, MODEL 516-8100 SERIES

The process interface controller is designed to interface the DDP-516 with the real-time environment of an industrial plant in applications such as data logging, supervisory control, direct digital control, etc. The process interface controller (PIC) decodes I/O instructions and connects selected I/O lines for data transfer, performs A/D and D/A conversions, controls logging and alarm typewriters, and isolates the DDP-516 from the control equipment to avoid damage to the computer from high voltage faults.

The PIC consists of a number of subsystems each of which performs one or more operations. These subsystems include:

a. Analog input subsystem
b. Digital input and output subsystem
c. Service subsystems
   (1) Timing chains
   (2) Logging typewriter
   (3) Customer interrupts

Physically, the PIC (Figure 5-12) consists of a group of racks each containing 1 to 3 nests of printed circuit cards. Within a nest the cards are arranged in two files one above the other. There are three different types of nests as follows:

a. Logic Nest. This nest, consisting of up to 24 cards per file, houses the service subsystems and the logic to interface the central processor with the other two subsystems.

b. Digital Input-Output Nest. This nest, consisting of up to 24 cards per file, houses the digital input/output subsystem. Cards in such a nest are addressed in pairs, with each card of a pair being above or below the other, with the two files of the nest. The card which plugs into a particular slot assumes the address of that slot.

c. Analog Input Nest. This nest, consisting of up to 22 cards per file, houses the analog input subsystem. Multiplexer cards are used in this nest and each cards contains six analog input points, i.e., connections to six analog input signals. These points assume the addresses corresponding to the slot into which the card is inserted.

The number of cards in a nest, the type of cards in a nest, and the number of nests in the PIC is determined by the system requirements.

The PIC is coupled to the DDP-516 mainframe by a device known as the process interface controller adapter (PICA) which supplies signal timing and synchronization for the PIC. A PICA is supplied with each PIC as part of the option and is physically mounted on the mainframe.

Programming

These instructions assigned to PIC are as follows:

OCP 'XX33	Acknowledge designated subsystem interrupt
SKS '0023	Skip if PIC is ready
SKS '0033	Skip if PIC is not interrupting

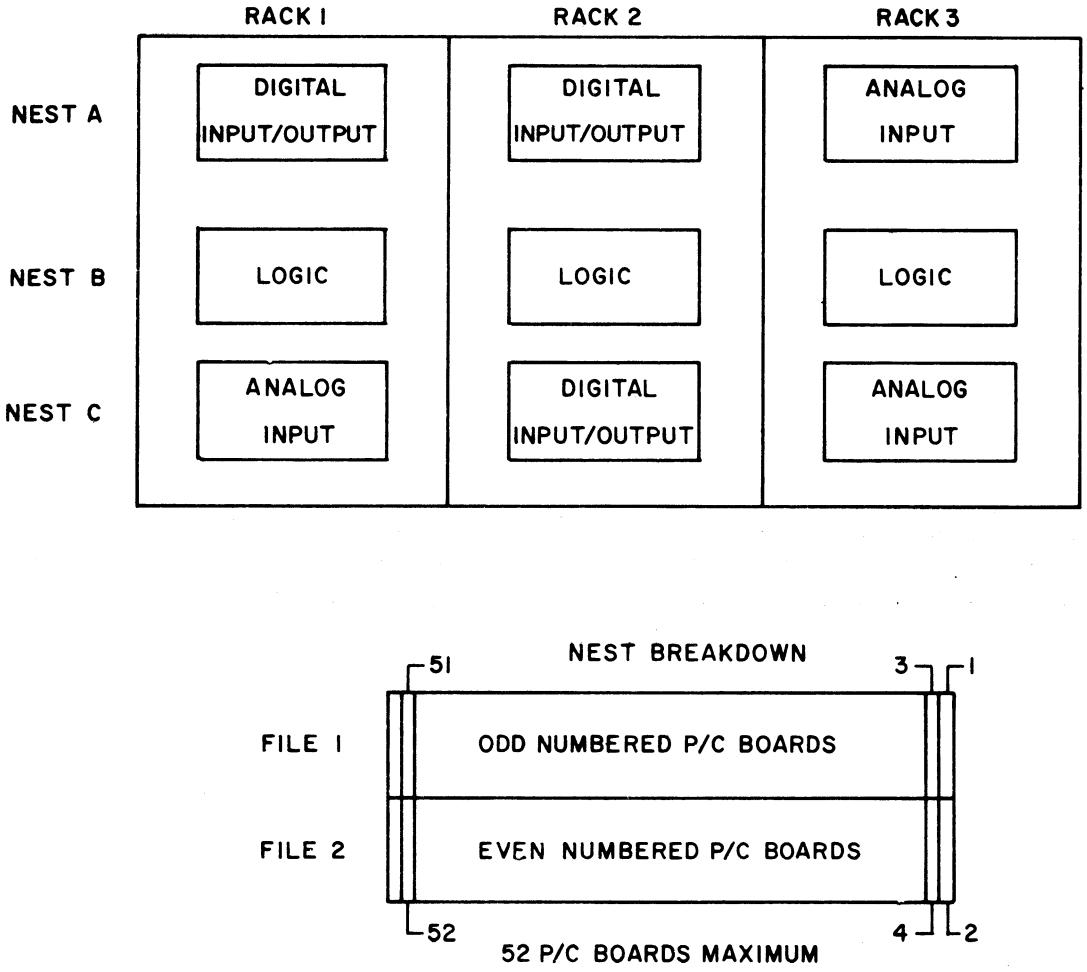


Figure 5-12. Typical 3-Rack, Extended RTCU and Nest Breakdown

SKS 'XX33	Skip if designated subsystem is Not interrupting
INA '0023	Input from PIC adapter if ready
INA '1023	Clear A-register and input from PIC adapter if ready
OTA '0123	Output select to PIC if ready
OTA '0323	Output data to PIC if ready
OTA '0723	Output and cycle PIC if ready
OTA '1033	Set PIC interrupt mask

The XX field in the OCP 'XX33 and SKS 'XX33 instructions specifies the PIC subsystem associated with the interrupt (see Table 5-11). Table 5-11 also specifies the bit positions in the A-register which must be set prior to executing an OTA '1033 instruction in order to enable the desired interrupts.

Table 5-11.
PIC Interrupt Designation

Subsystem	Contents of XX Field	A-Register Bit Position
Watchdog Timer	01 (Octal)	1 (Decimal)
Analog Input	02	2
Timing Chain A	03	3
Common Alarm	04	4
Counter Input	05	5
Customer Input 1	11	11
Customer Input 2	12	12
Timing Chain B	13	13
Timing Chain C	14	14
Logging Typewriter	15	15

Analog Input Subsystem

The analog input subsystem is capable of processing both high-level and low-level analog inputs. A high-level input can be in any one of four voltage ranges (±1, 5, 10, or 50 volts); a low-level input is ±50 mv. Full scale voltages in both levels are converted to ± 8191 by an A/D converter within the PIC.

An analog input nest contains up to 44 low-level addressable cards (model 516-8221) each of which services six analog input points. Thus a nest can accommodate 256 low-level points. (The unused points result from the octal addressing scheme.) A system can consist of up to four analog input nests for a total of 1024 low-level points. Only 1022 points are used since points 176 and 177 are reserved for check points. The high-level cards (model 516-8222) are similar in construction to the low-level cards except that there can be no more than 128 points in a system.

Card slots 5 through 48 in an analog input nest are addressed as $0\text{-}377_8$ in nest one, $400\text{-}777_8$ in nest two, $1000\text{-}1377_8$ in nest three, and $1400\text{-}1777_8$ in nest four. There are six analog input points per slot except for slots 47 and 48 which use only two points each. For each analog input card, the Initial Point (the point connected to terminals one and two) has the lowest address on that card. Refer to Table 5-12 and Figure 5-13 for the correspondence between the address of an analog input point, its card slot location, and the associated customer terminal location.

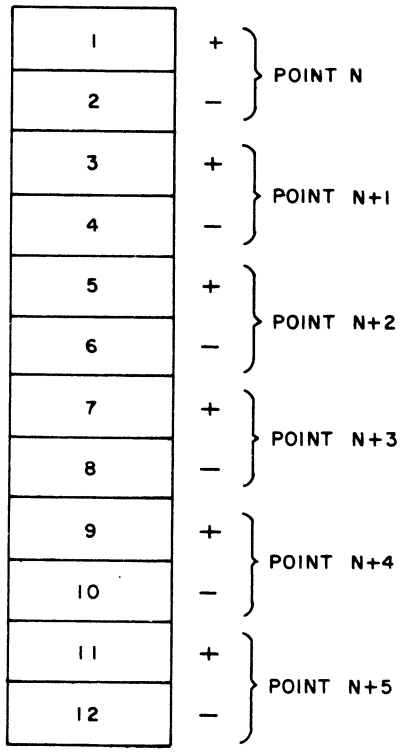


Figure 5-13. Terminal Connection/Point Address Correspondence

To convert an analog voltage or current to digital data and transfer this data to the central processor, the instructions listed on the following pages must be executed. The first two instructions select the desired analog input point, convert the corresponding signal to a digital value, and hold that value in the A/D converter.

Table 5-12.
Addresses of Initial Points for Analog Input Cards

Customer Connector Location	Card Slot Location	Octal Addresses of Initial Points			
		Nest 1	Nest 2	Nest 3	Nest 4
1	5	0000	0400	1000	1400
2	6	0200	0600	1200	1600
3	7	0006	0406	1006	1406
4	8	0206	0606	1206	1606
5	9	0014	0414	1014	1414
6	10	0214	0614	1214	1614
7	11	0022	0422	1022	1427
8	12	0222	0622	1222	1622
9	13	0030	0430	1030	1430
10	14	0230	0630	1230	1630
11	15	0036	0436	1036	1436
12	16	0236	0636	1236	1636
13	17	0044	0444	1044	1444
14	18	0244	0644	1244	1644
15	19	0052	0452	1052	1452
16	20	0252	0652	1252	1652
17	21	0060	0460	1060	1460
18	22	0260	0660	1260	1660
19	23	0066	0466	1066	1466
20	24	0266	0666	1266	1666
21	25	0074	0474	1074	1474
22	26	0274	0674	1274	1674
23	27	0102	0502	1102	1502
24	28	0302	0702	1302	1702
25	29	0110	0510	1110	1510
26	30	0310	0710	1310	1710
27	31	0116	0516	1116	1516
28	32	0316	0716	1316	1716
29	33	0124	0524	1124	1524
30	34	0324	0724	1324	1724
31	35	0132	0532	1132	1532
32	36	0332	0732	1332	1732
33	37	0140	0540	1140	1540
34	38	0340	0740	1340	1740
35	39	0146	0546	1146	1546
36	40	0346	0746	1346	1746
37	41	0154	0554	1154	1554
38	42	0354	0754	1354	1754
39	43	0162	0562	1562	1562
40	44	0362	0762	1362	1762
41	45	0170	0570	1170	1570
42	46	0370	0770	1370	1770
43	47	0176	0576	1176	1576
44	48	0376	0776	1376	1776

Table 5-13.
Digital Input-Output Addresses of Card Pairs

Card Pair Octal Address*		Customer Connection Location	Card Slot Locations
Upper Nest	Lower Nest		
00	40	1,2	5,6
01	41	3,4	7,8
02	42	5,6	9,10
03	43	7,8	11,12
04	44	9,10	13,14
05	45	11,12	15,16
06	46	13,14	17,18
07	47	15,16	19,20
10	50	17,18	21,22
11	51	19,20	23,24
12	52	21,22	25,26
13	53	23,24	27,28
14	54	25,26	29,30
15	55	27,28	31,32
16	56	29,30	33,34
17	57	31,32	35,36
20	60	33,34	37,38
21	61	35,36	39,40
22	62	37,38	41,42
23	63	39,40	43,44
24	64	41,42	45,46
25	65	43,44	47,48
26	66	45,46	49,50
27	67	47,48	51,52

*Counter inputs and common alarm inputs can be processed only via addresses 00 through 17 in rack 1. Alarm printer outputs and D/A outputs can be processed only via addresses 20 through 27 and 60 through 67.

To convert an analog voltage or current to digital data and transfer this data to the central processor, the instructions listed below must be executed. The first two instructions select a point, convert the selected data from analog form and hold the data in the A/D converter.

OTA '0123. -- This instruction specifies whether the input data is high or low level. When the instruction is executed, the A-register must contain

XX413Y,

where XX (bits 1 through 4) are unused and Y (bits 14 through 16) equals an octal 1 for a high-level input or an octal 2 for a low-level input. The PIC is busy for no more than two cycle times (1.92 μsec) after executing the instruction.

OTA '0323. -- This instruction transfers to the PIC the address of the desired analog input point. An OTA '0323 must be preceded somewhere in time by an OTA '0123 in order for the PIC Adapter on the main frame to transfer the address to the PIC. The address data format in the A-register must be

XXYYYY,

where XX (bits 1 through 4) is unused and YYYY (bits 5 through 16) specifies the octal address of the analog input point (see Table 5-12).

The PIC will be busy for no more than 11 cycle times (10.56 μsec) after executing this instruction. The instruction causes data from the addressed point to be converted. The conversion requires approximately 5 ms, and a standard interrupt is generated when the conversion is complete. During this interval the system is available to other operations except another analog input.

In response to the standard interrupt, instruction SKS '0233 is executed to determine whether an analog input is causing the interrupt. If the instruction does not skip, the analog input is in fact causing the interrupt and instruction OCP '0233 is executed to acknowledge the interrupt. Then instructions OTA '0723 and INA '1023 or INA '0023 must be executed before another analog input is requested.

OTA '0723. -- This instruction causes the converted data in the PIC to be transferred to the PIC adapter. In order for the transfer to take place, the A-register must contain

XX2200,

where XX (bits 1 through 4) are unused. The PIC is busy for no more than seven cycle times (6.72 μsec) after executing the instruction. The transfer does not clear the A/D register in the PIC.

INA '1023 and INA '0023. -- Instruction INA '1023 clears the A-register and transfers the data in the PIC adapter into bits 1 through 14 of the A-register. The value of the data from the A/D is in TWO's complement form:

$$-b_1 \cdot 2^{13} + \sum_{i=2}^{14} b_i \cdot 2^{14-i}$$

where b represetns bits 1, 2, ... 14 of register A. Thus, the plus full-scale value is 0774 and the minus full-scale value is 100004. Note that an arithmetic right shift by two bit positions will transform such data into a signed integer in the usual DDP-516 format. No I/O instructions having the device address 23 should be executed between an OTA '0723 and an INA '1023 or '0023. If this occurs, the analog input data will be lost.

An INA '0023 instruction is identical to an INA '1023 instruction except that the A-register is not cleared prior to the data transfer, the input data is ORed with the contents of the A-register and the result is retained in the register. The PIC is available for additional instructions at the conclusion of an INA '1023 or '0023.

Digital Input and Output Subsystem

A digital nest contains a maximum of 48 cards and, in general, each card services six bits of input or output data. Since each digital address is shared by a card pair, both cards in that pair must be either input or output types. A rack can contain two digital input/output nests which are designated as the upper nest and the lower nest. Card slots 5 through 52 in a nest are addressed in pairs as octal 00 through 27 in the upper nest and 40 through 67 in the lower nest. Refer to Table 5-14 for the correspondence between the address of a digital input or output and its card slot locations. Each of the A-register bit positions 5 through 16 is associated with a particular circuit on a pair of cards and the circuit in turn is associated with a particular input or output terminal pair. Refer to Table 5-14 for the correspondence between the A-register bits and the card connection terminal numbers.

Digital Inputs

There are three types of digital inputs available which are specified by the card configuration of the digital input/output nest. To process a particular input, the type of card capable of processing that input is inserted in the digital input/output nest. The digital input types are as follows.

a. Digital Levels. Model 516-8231, 32, 41, 42, 43. -- These inputs reflect the status of contacts or voltage levels. Upon command from the central processor, the status is input.

b. Common Alarms. Model 516-8233, 34, 35. -- These inputs reflect a change in process status which requires action by the central processor. The status change can be caused by contact or a voltage level. The data is input in a manner similar to a digital level

except that a standard interrupt is generated to notify the central processor of the change.

c. Counter Inputs. Model 516-8236, 37. -- These inputs constitue counts of contact closures or voltage pulses. The contents of any counter (6-bit capacity) can be transferred to the central processor upon command. The counter is automatically cleared to zero after such a transfer. When any one of the counters in the system is half full (32 counts), a standard interrupt is generated to permit reading before the counter overflows.

To process any digital inputs and transfer the data to the central processor the following instructions must be executed.

OTA '0723. -- This instruction transfers the address of the digital input to the PIC and transfers the input data to the PIC adapter. To accomplish the transfer, the A-register must contain

XX4YZZ,

where XX (bits 1 through 4) are unused, Y (bits 8 through 10) specifies the rack address (octal 1 or 2) and ZZ (bits 11 through 16) specifies the address of the digital input. See Table 5-7 for the correspondence between the ZZ field and the card slot numbers in a digital I/O nest. The PIC is busy for no more than 15 cycle times (14.4 μsec) after executing the instruction.

INA '1023 and INA '0023. -- Instruction INA '1023 clears A-register and transfers the input data into bits 5 through 16. (Bits 1 through 4 will contains zeros.) For digital input cards other than the counter-input type, the correspondence between bits read into the A-register and customer connection terminal numbers is given in Table 5-14.

Table 5-14.
Correspondence between A-register and Customer Connection Terminal Numbers

A-Register Bit	Card Position	Customer Connection Terminal Numbers*
5	Upper file	1, 2
6		3, 4
7		5, 6
8		7, 8
9		9, 10
10		11, 12
11	Lower file	1, 2
12		3, 4
13		5, 6
14		7, 8
15		9, 10
16		11, 12

*Provides for six inputs per card.

Counter input data will be transferred to the A-register in one of the following formats:

Counter Location	A-Register Bit 5	6	7	8	9	10	11	12	13	14	15	16
counter in lower file	Data from other Card						C_5	C_4	C_3	C_2	C_1	C_0
counter in upper file		C_5	C_4	C_3	C_2	C_1	C_0	Data from other Card				
counter in both files		C_5	C_4	C_3	C_2	C_1	C_0	C_5	C_4	C_3	C_2	C_1	C_0

For any such counter, the number of counts equals

$$\sum_{i=0}^{5} C_i \quad 2^i,$$

No I/O instructions having the device address 23 should be executed between an OTA '0723 and an INA '1023 or '0023. If this occurs, the input data will be lost. For level or alarm inputs this may not be critical, but for counter inputs the data is irrevocably lost because counters are cleared following the data transfer.

The INA '0023 instruction is identical to an INA '1023 except the A-register is not cleared, the input data is ORed with the current contents of the register, and the result retained in the register.

In response to an interrupt, instruction SKS '0433 (common alarm) or SKS '0533 (counter half full) is executed to determine whether the designated input is causing the interrupt. If the instruction does not skip, the designated input is causing the interrupt and instruction OCP '0433 or OCP '0533 must be executed to acknowledge an interrupt. Any further refinement in determining the source of the interrupt must be based on scanning the relevant input data for changes in value.

Digital Outputs

Several types of digital output cards are available and are described below (a through g). References to addressing pertain to the discussion under OTA '0123. References to positions in the A-register apply to the text under OTA '0323.

a. Single-Shot (Models 516-8301 trhough 8309. -- A single-shot output circuit is set when the card containing the circuit is addressed and the associated bit position in the A-register is a ONE. The circuit remains set for a specific time interval and cannot be reset by program action. If the circuit is readdressed before the time interval has elapsed, the output pulse width is undefined. Refer to Table 5-15 for a list of the single-shot circuits by model number and the time interval associated with each circuit.

b. Clamp (Models 516-8321 through 8332). -- A clamp output circuit functions in a manner similar to the single-shot circuit. Refer to Table 5-15 for a list of the clamp circuits by model number and the time interval associated with each circuit.

c. Flip-Flop (Model 516-8335). -- A flip-flop output circuit is set when addressed when the associated bit position in the A-register equals a ONE. The circuit remains set until addressed again with the A-register bit position set to ZERO.

d. Relay (Model 516-8336). -- A relay output circuit functions similar to a flip-flop circuit except that when the flip-flop is set a relay contact is closed and when reset the contact is opened.

e. Alarm Printer (Model 516-8151). -- When addressed, this output circuit services up to two RO-35 teletype units which type the same information at a rate of 10 characters per second, maximum. The teletype utilizes a slightly modified version of ASCII code (see Table 5-16) and up to 72 characters can be typed on a line. A system can service up to 32 teletype units.

f. D/A Converter (Models 516-8342 through 8346). -- When addressed, this output card pair generates a voltage or current proportional to the digital value transferred to it from the central processor. The system is capable of handling up to 32 analog outputs.

g. Stepping Motor Driver (Model 516-8351). -- When addressed, this output drives three stepping motors at a 200 step per second rate. There must be a 5 ms delay between each stepping command or the resulting action will be undefined. A complete revolution is accomplished by 200 commands in the same direction.

Table 5-15.
Output Circuit Delay Times

Single-Shot		Clamp	
Model No.	Time, ms	Model No.	Time, ms
516-8301	3.95	516-8321	1.00
516-8302	10.00	516-8322	3.10
516-8303	23.00	516-8323	10.00
516-8304	39.50	516-8324	18.40
516-8305	69.00	516-8325	31.00
516-8306	100.00	516-8326	55.50
516-8307	230.00	516-8327	100.00
516-8308	470.00	516-8328	217.00
516-8309	1000.00	516-8329	455.00
		516-8330	1000.00

To output digital data from the central processor to the PIC, the following instructions must be executed.

OTA '0123. -- This instruction transfers to the PIC the address of the desired output card pair. The address data format in the A-register must be

XX4YZZ

where XX (bits 1 through 4) are unused, Y (bits 8 through 10) specifies the rack address (octal 1 or 2) and ZZ (bits 11 through 16) specifies the address of the output. See Table 5-13 for the correspondence between the ZZ field and the card slot numbers in a digital I/O nest. The PIC is busy for no more than two cycle times (1.92 μsec) after executing the instruction.

OTA '0323. -- This instruction transfers the output data to the PIC. An OTA '0323 must be preceded by an OTA '0123 in order for the transfer to take place. The format of the data in the A-register when this instruction is executed must be

XXYYYY

where XX (bits 1 through 4) are unused and in general each bit of YYYY (bits 5 through 16) is associated with a customer terminal number (see Table 5-14). The PIC is busy for no more than 11 cycle times (10.56 μsec) after executing this instruction. No I/O instructions having a device address 23 are permitted between OTA '0123 and an OTA '0323.

When the output data is destined for the alarm printer, a special format is required in the A-register. Moreover, the absence of a ready interlock on the alarm printer means that this instruction can transfer data even when the printer is not ready. This necessitates the use of an auxiliary timing facility to accommodate the 10 character per second typing rate. The data format in the A-register is

Bit Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Data	0	0	0	0	0	b_6	b_5	b_4	b_3	b_2	b_1	b_0	1	0	0	0

where b_0-b_6 (bits 6 through 12) is a modified ASCII code. Refer to Table 5-16 for a list of the codes (characters and function) recognized by the alarm printer output cards.

Table 5-16.
Alarm Printer Codes

Code	Character or Function	Code	Character or Function	Code	Character or Function
0230	H TAB	1450	2	2230	I
0250	LF	1470	3	2250	J
0330	CR	1510	4	2270	K
0350	SO	1530	5	2310	L
0370	SI	1550	6	2330	M
1010	Space	1570	7	2350	N
1030	≥ *	1610	8	2370	O
1050	"	1630	9	2410	P
1070	#	1650	:	2430	Q
1110	$	1670	;	2450	R
1130	%	1710	<	2470	S
1150	Δ *	1730	=	2510	T
1170	∇ *	1750	>	2530	U
1210	(	1770	?	2550	V
1230	)	2010	← *	2570	W
1250	*Asterisk	2030	A	2610	X
1270	+	2050	B	2630	Y
1310	, Comma	2070	C	2650	Z
1330		2110	D	2670	≤ *
1350	. Period	2130	E	2710	\
1370	/	2150	F	2730	]
1410	0	2170	G	2750	↑
1430	1	2210	H	2770	←

*Modification of ASCII Code

When the output data is being supplied to a D/A converter, the data format in the A-register is slightly different from the general format. Bits 1 through 6 are not used and bits 7 through 16 must contain octal appropriate to the D/A output card pair involved. Refer to Table 5-17 for these octal values, the associated model numbers, and their analog outputs.

There are two bits in the A-register associated with each of the stepping motors. One bit represents forward motion, the other reverse motion. If both bits are zero, the motor is not stepped. If either bit is a ONE, the motor is stepped in the appropriate direction.

If both bits are ONE, the motor action is undefined. Refer to Table 5-18 for the correspondence between the bits in the A-register during an OTA '0323, the motor stepped, and its direction. In Table 5-18, motors 1, 2, and 3 are connected to terminal 1-4, 5-8, and 9-12, respectively.

Table 5-17.
D/A Outputs

Card Option	Value in A-Register			
	0000_8	0001_8	1000_8	1777_8
516-8342		-10	0v	+10v
516-8343	0v			+10v
516-8344	-10v			0v
516-8345	0 ma			20 ma
516-8346	0 ma			50 ma

Table 5-18.
Stepping Motor Command Bits

Motor	Direction	A-Register Bits	
		Upper File	Lower File
1	Forward	5	11
1	Reverse	6	12
2	Forward	7	13
2	Reverse	8	14
3	Forward	9	15
3	Reverse	10	16

Service Subsystems

There are three service subsystems associated with the PIC which are as follows.

a. Timing Chains Subsystem
b. Logging Typewriter Subsystem
c. Customer Interrupts Subsystem

Timing Chains. -- There are four timing chains available, the watchdog timer and three customer timing chains. All timing chains are retriggerable timing devices which can be initiated by the central processor via instruction OTA '0123. The contents of the A- register specify the chain involved. Each time that instruction is executed, the timing cycle restarts. If the instruction is not received within a specific interval, the device times out and an interrupt is generated. Each chain has one or more time delays which are selected at system makeup time. Once selected, the delays are variable within specified limits by mechanical adjustment. Refer to Table 5-19 for the values to be loaded into the A-register to select a timing chain and its associated delay.

Table 5-19
Timing Chain Designation

Timing Chain	(A)	Delay
Watchdog	2405	1.0 to 10 sec
A	2403	0.1 to 1 ms 3.0 to 30 ms 30 to 300 ms
B	2406	0.6 to 6.0 ms 0.1 to 1.0 sec 1.0 to 10 sec
C	2411	0.1 to 1.0 m* 3.0 to 30 m 30 to 300 m

*Timing chain C is always set to 100 ms when alarm typewriter is included in the system.

If one of the timing devices causes an interrupt, instructions SKS 'XX33 and OCP 'XX33 must be executed to determine which device is causing the interrupt and acknowledge the associated interrupt. For the XX values of each timing chain, refer to Table 5-11.

Logging Typewriter, Models 516-8161 through 8172. -- The logging typewriter subsystem consists of from one to five typewriters and two output cards which are mounted in the digital input/output nest. The addressing of the connector slots containing the cards and the transferring of data are the same as for any output card pair. Any combination of one to five typewriters may print information simultaneously. During the data transfer operation (see OTA '0323 below), any combination of logging typewriters connected to the associated card pair may be designated as active. The character being transferred will then be typed simultaneously by all active typewriters. The typewriters are capable of printing up to 10 characters per second and the carriage width can be 20, 24, or 30 inches (14 characters per inch).

To output data to the logging typewriter, instruction OTA '0123 is executed with the contents of the A-register equal to:

XX2414,

where XX (bits 1 through 4) are unused. Instruction OTA '0123 is executed again with the A-register containing the rack number and address of the output card pair. Then the data is transferred via instruction OTA '0323 with the data in the A-register. Bits 1 through 5 are unused, bits 6 through 10 indicate which typewriter(s) are to be used (one bit for each typewriter) and bits 11 through 16 contain the code for the character to be typed or function to be performed. Table 5-20 contains a list of the characters or functions and the associated octal codes.

Table 5-20.
Logging Typewriter Character Codes

Character	Octal Code	Character	Octal Code
A	01	Y	31
B	02	Z	32
C	03	Horizontal Tab	34
D	04	Carriage Return	35
E	05	Shift Black	36
F	06	Shift Red	37
G	07	Space	40
H	10	#	43
I	11	$	44
J	12	%	45
K	13	&	46
L	14	,	54
M	15	-	55
N	16	.	56
O	17	0	60
P	20	1	61
Q	21	2	62
R	22	3	63
S	23	4	64
T	24	5	65
U	25	6	66
V	26	7	67
W	27	8	70
X	30	9	71

Following a data transfer, a standard interrupt will occur which must be tested via an SKS '1533 instruction. Then, if the logging typewriter caused the interrupt, an OCP '1533 must be executed to acknowledge the interrupt. The interrupt occurs 100 ms after a data transfer unless a horizontal tab or a carriage return had been transmitted. If either of these functions had been transmitted, the interrupt will not occur until approximately 1 sec after the transfer. Since the logging typewriter is not equipped with a ready interlock, the above-described interlock-driven method of I/O transfer must be used.

Customer Interrupts. -- The PIC provides the buffering contact closer signals directly to the standard interrupt line. Two terminals per system are provided for this purpose. Instructions SKS '1133 or '1233 and the OCP '1133 or '1233 are applicable to the two associated customer interrupt conditions.

Sample Programs

This subroutine inputs one low-level analog input. During the 5 ms multiplexing interval, additional processing can be performed provided that it does not include another analog input. When multiplexing is complete, program control returns to this subroutine via an interrupt subroutine.

```
            REL
            SUBR    AIN         Establish subroutine name
AIN         DAC     **          Return address
            LDA     ='4132      Specify low-level analog input
            OTA     '0123       Output select if PIC ready
            JMP     *-1         Wait till ready
            LDA     ='200       Specify point address
            OTA     '0323       Output address if PIC ready
            JMP     *-1         Wait till ready
            JMP*    AIN         Return to caller until multiplexing complete

            5-ms interval

BACK        DAC     **          Return address
            SKS     '0033       PIC interrupting?
            JMP     *+2         Yes
            JMP*    BACK        No. Return to interrupt routine
            SKS     '0233       Analog input interrupting?
            JMP     *+2         Yes
            JMP*    BACK        No. Return to interrupt routine
            OCP     '0233       Acknowledge interrupt
            LDA     '2200       Specify A/D transfer
            OTA     '0723       Input data to pica if PIC ready
            JMP     *-1         Wait till ready
            INA     '1023       Clear A and input data if PIC ready
            JMP     *-1
            STA     BUF         Store input
            JMP*    BACK        Return to interrupt routine
BUF         BSS     1
            END
```

This subroutine inputs one digital level and stores the input. Following some internal processing, the subroutine sets a flip-flop to indicate that the input has been received and processed.

```
        REL
        SUBR    DIO
DIO     DAC     **
        LDA     '4117       Specify input address - Rack 1
                            Address 17 octal
        OTA     '0723       Output the address if PIC ready
        JMP     *-1         Wait till ready
        INA     '1023       Input digital level if PIC ready
        JMP     *-1         Wait till ready
        STA     BUFA        Store input

        Process Data and Determine Output

        LDA     '4217       Specify output address - rack 2
                            address 17 octal
        OTA     '0123       Output the address if PIC ready
        JMP     *-1         Wait till ready
        LDA     '400        Specify output flip-flop to be set
        OTA     '0323       Output data if PIC ready
        JMP     *-1         Wait till ready
        JMP*    DIO         Return to caller
BUFA    BSS     1
        END
```

SECTION VI
OPERATION

CONTROL CONSOLE

A separate console unit containing all operating controls and indicators is provided in each DDP-516 system. The console control panel is illustrated in Figure 6-1; the controls and indicators which it contains are described in Table 6-1.

OPERATING PROCEDURES

Turn-On, Turn-Off

To turn on the computer, depress the control panel POWER-ON indicating pushbutton. This operation will apply primary input power to the system and will normalize the status of the machine.

The POWER-ON indicating pushbutton is illuminated when dc power is applied to the memory.

To turn off the computer, depress the control panel POWER-OFF pushbutton. All input power to the system will be removed upon the operation of this control.

Initialize System

When desired, the computer may be initialized by depressing the control panel MSTR CLEAR pushbutton. The operation of this control clears registers A, B, E, M, F, P, Y, and SC. All timing levels are set to the state which would exist after the execution of a HALT (HLT) instruction (timing level 3 of FETCH cycle).

The operation of the MASTER CLEAR control affects neither the memory nor the X-register of the system.

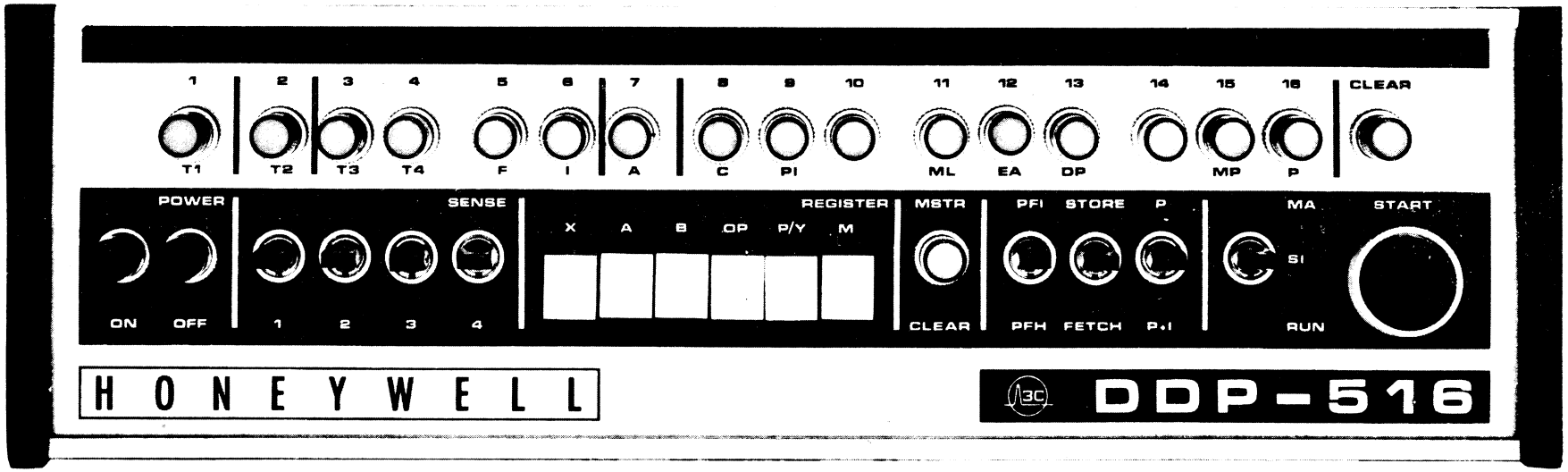


Figure 6-1. Control Console, Control Panel

Table 6-1.
Control Panel Controls and Indicators

Panel Designation	Normal Position	Type	Function
1, 2,...15, 16	NA	Indicating Pushbuttons	This control is used for the display of the contents of each bit position of a selected CPU register, for the manual bit-by-bit entry of data bits into the selected register and the display of the states of key control flip-flops.
		NOTE These indicators have two sets of panel symbols (upper and lower); those listed in this table (upper set) and those listed in Table 7-2.	
DATA CLEAR	NA	Pushbutton	This control clears any selected (A, B, P/Y, M) register.
START	NA	Indicating Pushbutton	This control implements the step-by-step reading or insertion of data into consecutive memory locations and for the step-by-step execution of programs. The indicator is illuminated to indicate a RUN condition.
SENSE, 1, 2, 3, 4	OFF	Two-Position Toggle Switches (4 ea)	These switches, operated with corresponding skip instructions in the computer repertoire, enable the operator to initiate a skip instruction to select and/or alter the course of a program during its execution.
MA/SI/RUN	RUN	Three-Position Toggle Switch	This switch enables the operator to select the operating mode of the computer. The modes selected by each switch position are as follows: 1) MA, Memory Access mode during which data may be read and displayed from or inserted into a memory word location. 2) SI, Single Instruction mode which permits the step-by-step execution of a program. 3) RUN, Normal computer operating mode during which the performance of a program may be stopped either by the execution of a HALT (HLT) instruction or by the positioning of the mode selector switch to any of the other two positions. MSTR CLEAR, DATA CLEAR and indicating push-buttons 1-16 are disabled in this (RUN) position.

Table 6-1. (Cont)
Control Panel Controls and Indicators

Panel Designation	Normal Position	Type	Function
STORE/FETCH	FETCH	Two-Position Lever-Type Switch	In the FETCH position, this switch permits the readout and display of an addressed memory word location. In the STORE position, this switch enables the insertion of data into an addressed memory word location. If the MA/SI/RUN switch is in SI or RUN mode, the STORE/FETCH switch is disabled.
PFI/PFH	PFH	Two-Position Lever-Type Switch	Used to determine the operation performed by the computer on the detection of power failure. The operation for each position is: 1) PFI, the computer will execute a program interrupt when power fails. 2) PFH, the computer will stop when power fails.
P/P+1	P+1	Two-Position Lever-Type Switch	In the P position this switch, in conjunction with other controls and indicators, permits the operator to address and read data from or write data into an addressed memory word location. In the P+1 position, this switch permits the development of consecutive memory location addresses by causing the previous address to be incremented by one. If the MA/SI/RUN switch is in the SI or RUN mode, the P/P+ 1 switch is disabled.
REGISTER, X, A, B, OP, P/Y, M	OP	Six Interlocked Pushbuttons	The operation of keys A, B, X, and M cause the contents of the corresponding main frame registers to be displayed at the control panel. The operation of key P/Y causes the contents of the main frame Y register to be displayed at the control panel. If the computer is in an MA mode, the main frame Y and P registers contain the same data; however, in the SI mode the P register contains one more than the Y register. In either case, only the Y register is displayed. The selection of the OP control key causes the states of key control flip-flops to be displayed (refer to Display Operational Data Procedure).

Table 6-1. (Cont)
Control Panel Controls and Indicators

Panel Designation	Normal Position	Type	Function
MSTR CLEAR	NA	Pushbutton	When operated, this control places the computer in a standard cleared state in which registers A, B, M, P, and Y are cleared; the clock is stopped; and all timing registers are set to the condition which would exist following the execution of a HALT (HLT) instruction. The operation of this control has no effect on memory or the X register.
POWER ON	NA	Indicating Pushbutton	The operation of this control applies primary power to the computer. The control is illuminated when dc power for the memory is on.
POWER OFF	NA	Pushbutton	The control, when operated, removes primary power from the computer.

Table 6-2.
Control Panel Data Bit Indicators
Displayed Operational Functions and Indicator Symbols

Applicable Indicator Symbols	Bit Number	Function
T1	1	Timing Level 1
T2	2	Timing Level 2
T3	3	Timing Level 3
T4	4	Timing Level 4
F	5	Fetch Cycle, F
I	6	Indirect Cycle, I
A	7	Execute Cycle, A
C	8	C Bit
PI	9	Permit Interrupt, Indicator illuminated when interrupt permitted
--	10	Unassigned
ML	11	Restricted Mode (Memory Lockout Option)
EA	12	Extended Mode (24K or 32K memory)
DP	13	Double Precision (DP) mode (High-Speed Arithmetic Option)
--	14	Unassigned
MP	15	Memory Parity Error (Memory Parity Option)
P	16	I/O Parity Error (utilized with options which provide parity checking)

NOTE

The operation of the MSTR CLEAR pushbutton will reset all indicators except Timing Level 3 (Bit 3) and Fetch Cycle (Bit 5) which will be set.

Read Single Memory Location

The procedure required to access a single memory word location and display the 16-bit contents of the location at the control panel is as follows:

1) Set MODE switch to MA.
2) Set FETCH/ STORE switch to FETCH.
3) Set P/P+1 switch to P.
4) Depress P/ Y REGISTER control button.
5) Operate CLEAR pushbutton.
6) Enter desired memory word location address using data bits indicating pushbuttons (3-16).
7) Depress M REGISTER control button.

8) Operate START pushbutton

9) View data bits indicating pushbuttons for desired display

Read Consecutive Memory Locations

To read a series of successive memory word locations without being required to address each location individually, perform the above procedure required to read the first location. Then:

10) Set the P/P+1 switch to P+ 1

11) The START pushbutton must be operated each time that a succeeding location is to be displayed

NOTE

To display at any time (via DATA BITS indicating pushbuttons) the address of the memory location last read from, depress the P/Y REGISTER control pushbutton.

Single Memory Location Data Insertion and/or Modification

The procedure required to access a single memory word location and to enter data into or modify the contents of the location is as follows:

1) Set MODE switch to MA

2) Set FETCH/STORE switch to STORE

3) Set P/P+1 switch to P

4) Depress P/Y REGISTER control button

5) Operate CLEAR pushbutton

6) Enter desired memory word location address using data bits indicating pushbuttons (3-16)

7) Depress M REGISTER control button

8) Enter desired word or modification bits using data bits indicating pushbuttons

9) Operate START pushbutton to complete operation

NOTE

Whenever information is written into location 00000, the same information is copied into the X register. The contents of this register may be displayed by depressing the X SELECT control button but may be changed only by writing into location 00000.

Consecutive Memory Location Data Insertion And/Or Modification

To insert the same word or modification bits into a series of successive memory locations without being required to address each location individually, perform the above procedure required for the first word. Then:

10) Set the P/P+1 switch to P+1

11) The START pushbutton must be operated to initiate each successive data insertion

NOTE

To display at any time (via data bits indicating pushbuttons) the address of the memory location last written into, depress the P/Y REGISTER control button.

Single-Step Program Execution

A stored program may be examined in detail by executing it step-by-step in the following manner:

1) Set MODE switch to SI
2) Operate MSTR CLEAR pushbutton
3) Select desired register using REGISTER control buttons A, B, or P/Y
4) Enter desired initial values using data bits indicating pushbuttons
5) Operate START pushbutton. This causes the first instruction to be fetched and loaded into the M register. The display of the first instruction is obtained by the operation of REGISTER control button M. After the first instruction, each time the START pushbutton is operated the previously fetched instruction is executed, the next instruction is fetched, the P register is incremented, and the computer stops. The operation of REGISTER control button P/Y at this time will cause the data bits indicators to display the Y register which will contain the address from which the new instruction was fetched. Note that the P register, which is not displayed, will contain a value one higher than that in the Y register.

Read Mainframe Register

To display the contents of mainframe registers A, B, X, Y, or M at the control panel depress the corresponding REGISTER button. Bits 1 through 16 of the selected register will be displayed by the control panel data bits (1 through 16) indicating pushbuttons. An illuminated indicator designates a ONE bit an unlighted indicator a ZERO bit.

Display Operational Data

The operation of the OP REGISTER control button causes the operational status of circuits within the computer to be displayed by the control panel data bits indicators. The functional status indicated by each of the 16 indicating pushbuttons and the symbol applicable to each when displaying operation data are described in Table 7-2.

Run Program

To enable the computer to perform a program in its normal RUN mode, do the following:

1) Set MODE switch to RUN
2) Operate MSTR CLEAR pushbutton
3) Depress P/Y REGISTER control button
4) Enter Starting address using the DATA BITS indicating pushbuttons 1 - 16.

NOTE

If this is a program restart procedure, it may be necessary to modify or enter new data into other registers of the computer at this time. The procedure would be to operate the appropriate REGISTER control button and enter the necessary data using the data bits controls.

5) Set MODE switch to RUN
6) Operate START pushbutton to initiate automatic execution of program. The selected program will run until either a HLT (halt) instruction is performed or the MODE control switch is set to the SI position. In either case, the computer is stopped in a standard operating condition and can be restarted in either the RUN or SI mode.

Manual Instruction Insertions

Categorization of Repertoire. -- Instructions in the left column may be executed from the M-register without access to memory. Instructions in the right column will not operate correctly under these conditions.

1. I/O and Mode Control

OCP -	INA
SMK (N) -	OTA
ENB -	HLT
INH -	
and, with options	
RMP -	
SGL -	
DBL -	
ERM -	
EXA -	
DXA -	

2. Register and Memory Change

LDA, STA } not double precision	JST
	IMA
ADD IAB	CAS
SUB RCB	IRS
ANA SCB	LDX
ERA CSA	SKS
CRA JMP	all SHifts
SSP all Skips	CHS
SSM	CMA
AOA and, with option	TCA
ACA MPY	
CAL SCA	DIV
CAR	NRM
ICL	
ICR	
ICA	
STX	

APPENDIX A
NUMBERING SYSTEM AND TWO'S COMPLEMENT ARITHMETIC

Binary Numbering System

Sixteen-bit data words are stored in two's complement notation. The most significant bit of a data word may be considered to be the arithmetic sign of the number represented. The MSB is ZERO for positive (+) numbers and a ONE for negative (-) numbers. Bits 2 through 16 of the data word represent the value in binary form. Positive values thus range from zero (which always has a positive sign) to 32,767 as follows:

0	000 000 000 000 000	Zero
0	000 000 000 000 001	+1
0	000 000 000 000 010	+2
	'	'
	'	'
	'	'
	'	'
0	111 111 111 111 111	+32,767

Negative numbers are represented in two's complement form and always have a ONE in the sign bit position.

Two's Complement Arithmetic

The two's complement of a binary number is obtained by complementing (reversing) each bit and adding one. For example, the two's complement of +1, which represents -1, is obtained as follows:

+1	0	000 000 000	000 001
Complement	1	111 111 111	111 110
Add 1	0	000 000 000	000 001
Two's Complement (-1)	1	111 111 111	111 111

The number range for negative values is from -1 to -32,768 as follows:

1	111 111 111 111	111	(-1)
1	111 111 111 111	110	(-2)
1	111 111 111 111	101	(-3)
1	000 000 000 000	000	(-32,768)

If + 1 is added to -1, the result is zero. Thus:

1	111 111 111 111	111	-1
0	000 000 000 000	001	+1
0	000 000 000 000	000	Zero

Note that a carry bit from the most significant position has been ignored. In two's complement arithmetic, if numbers of unlike signs are added together, carries from the most significant bit are disregarded.

Overflow

Overflow is the condition that occurs when two numbers of like signs are added together to produce a sum of a different sign. For example, adding +1 to ±32,767 would produce a result larger than the capacity of a single data word.

0	111 111 111 111	111	(+32,767)
0	000 000 000 000	001	(+1)
1	000 000 000 000	000	

The different sign of the result defines an overflow condition.

Addition on the computer is performed by adding a quantity in the memory to a quantity in the A-register. True signed arithmetic takes place. Overflow conditions automatically result in the setting of the C-bit indicator, even though no carry is propagated from the sign position. In the preceding example, the C-bit indicator would be set.

APPENDIX B
DDP-516 PERIPHERAL DEVICE CODES

Character	ASCII Code*	Card Code		Mag Tape Code
		Hollerith	Octal	
0	260	0	12	12
1	261	1	01	01
2	262	2	02	02
3	263	3	03	03
4	264	4	04	04
5	265	5	05	05
6	266	6	06	06
7	267	7	07	07
8	270	8	10	10
9	271	9	11	11
A	301	12-1	61	61
B	302	12-2	62	62
C	303	12-3	63	63
D	304	12-4	64	64
E	305	12-5	65	65
F	306	12-6	66	66
G	307	12-7	67	67
H	310	12-8	70	70
I	311	12-9	71	71
J	312	11-1	41	41
K	313	11-2	42	42
L	314	11-3	43	43
M	315	11-4	44	44
N	316	11-5	45	45
O	317	11-6	46	46
P	320	11-7	47	47
Q	321	11-8	50	50
R	322	11-9	51	51
S	323	D-2	22	22
T	324	D-3	23	23
U	325	D-4	24	24
V	326	D-5	25	25
W	327	D-6	26	26
X	330	D-7	27	27
Y	331	D-8	30	30
Z	332	D-9	31	31
Space	240	Blank	20	20
!	241[2]	8-6	16	16
"	242[2]	0-8-7	37	37
#	243[2]			
$	244[2]	11-8-3	53	53
%	245[2]	12-8-5	75	75
&	246[2]			
'	247[2]	8-4	14	14
(	250[2]	0-8-4	34	34
)	251[2]	12-8-4	74	74
*	252[2]	11-8-4	54	54
+	253[2]	12	60	60
,	254	0-8-3	33	33
—	255	11	40	40
.	256	12-8-3	73	73
/	257	01	21	21
:	272	8-5	15	15
;	273	11-8-2	52	52
<	274[2]		57	57
=	275[2]		13	13
>	276[2]		17	17
?	277[2]			
@	300[2]			
[	333[3]	11-8-5	55	55
\	334[4]	12-8-6	76	76
]	335[5]	0-8-6	36	36
↑	336[6]	12-8-2	72	72
←	337	12-8-7	77	77

*Used by ASR and Line Printer

APPENDIX C
SUMMARY OF STANDARD INSTRUCTIONS
(Listed in Alphabetical Order)

Mnemonic	Octal Code	Instruction	Type	Execution Time (μsec)	Page
ACA	141216	Add C to A	G	0.96	2-3
ADD	06	Add	MR	1.92	2-3
ALR	0416	Logical Left Rotate	SH	0.96 + 0.48n	2-4
ALS	0415	Arithmetic Left Shift	SH	0.96 + 0.48n	2-4
ANA	03	AND to A	MR	1.92	2-4
AOA	141206	Add One to A	G	0.96	2-3
ARR	0406	Logical Right Rotate	SH	0.96 + 0.48n	2-5
ARS	0405	Arithmetic Right Shift	SH	0.96 + 0.48n	2-5
CAL	141050	Clear A, Left Half	G	0.96	2-12
CAR	141044	Clear A, Right Half	G	0.96	2-12
CAS	11	Compare	MR	2.88	2-10
CHS	140024	Complement A Sign	G	0.96	2-4
CMA	140401	Complement A	G	0.96	2-4
CRA	140040	Clear A	G	0.96	2-3
CSA	140320	Copy Sign and Set Sign Plus	G	0.96	2-4
ENB	000401	Enable Program Interrupt	G	0.96	2-10
ERA	05	Exclusive OR to A	MR	1.92	2-4
HLT	000000	Halt	G		2-10
IAB	000201	Interchange A and B	G	0.96	2-3
ICA	141340	Interchange Characters in A	G	0.96	2-12
ICL	141140	Interchange and Clear Left Half of A	G	0.96	2-13
ICR	141240	Interchange and Clear Right Half of A	G	0.96	2-13
IMA	13	Interchange Memory and A	MR	2.88	2-3
INA	54	Input to A	IO	1.92	2-9
INH	001001	Inhibit Program Interrupt	G	0.96	2-10
INK	000043	Input Keys	G	0.96	2-3
IRS	12	Increment, Replace and Skip	MR	2.88	2-11
JMP	01	Unconditional Jump	MR	0.96	2-11
JST	10	Jump and Store Location	MR	2.88	2-11
LDA	02	Load A	MR	1.92	2-3
LDX	15	Load X	MR	2.88	2-3
LGL	0414	Logical Left Shift	SH	0.96 + 0.48n	2-5

APPENDIX C (Cont)
SUMMARY OF STANDARD INSTRUCTIONS
(Listed in Alphabetical Order)

Mnemonic	Octal Code	Instruction	Type	Execution Time (μsec)	Page
LGR	0404	Logical Right Shift	SH	0.96 + 0.48n	2-5
LLL	0410	Long Left Logical Shift	SH	0.96 + 0.48n	2-6
LLR	0412	Long Left Rotate	SH	0.96 + 0.48n	2-6
LLS	0411	Long Arithmetic Left Shift	SH	0.96 + 0.48n	2-7
LRL	0400	Long Right Logical Shift	SH	0.96 + 0.48n	2-7
LRR	0402	Long Right Rotate	SH	0.96 + 0.48n	2-8
LRS	0401	Long Arithmetic Right Shift	SH	0.96 + 0.48n	2-8
NOP	101000	No Operation	G	0.96	2-11
OCP	14	Output Control Pulse	IO	1.92	2-9
OTA	74	Output From A	IO	1.92	2-9
OTK	171020	Output Keys	IO	1.92	2-3
RCB	140200	Reset C Bit	G	0.96	2-11
SCB	140600	Set C Bit	G	0.96	2-11
SKP	100000	Unconditional Skip	G	0.96	2-11
SKS	34	Skip if Ready Line Set	IO	1.92	2-10
SLN	101100	Skip if (A_{16}) is ONE	G	0.96	2-11
SLZ	100100	Skip if (A_{16}) is ZERO	G	0.96	2-11
SMI	101400	Skip if A Minus	G	0.96	2-11
SMK	74	Set Mask	IO	1.92	2-10
SNZ	101040	Skip if A Not ZERO	G	0.96	2-11
SPL	100400	Skip if A Plus	G	0.96	2-11
SRC	100001	Skip if C Reset	G	0.96	2-12
SR1	100020	Skip if Sense Switch 1 is Reset	G	0.96	2-11
SR2	100010	Skip if Sense Switch 2 is Reset	G	0.96	2-11
SR3	100004	Skip if Sense Switch 3 is Reset	G	0.96	2-11
SR4	100002	Skip if Sense Switch 4 is Reset	G	0.96	2-12
SSC	101001	Skip if C Set	G	0.96	2-12
SSM	140500	Set Sign Minus	G	0.96	2-4
SSP	140100	Set Sign Plus	G	0.96	2-4
SSR	100036	Skip if no Sense Switch Set	G	0.96	2-12
SSS	101036	Skip if any Sense Switch is Set	G	0.96	2-12
SS1	101020	Skip if Sense Switch 1 is Set	G	0.96	2-12
SS2	101010	Skip if Sense Switch 2 is Set	G	0.96	2-12
SS3	101004	Skip if Sense Switch 3 is Set	G	0.96	2-12
SS4	101002	Skip if Sense Switch 4 is Set	G	0.96	2-12
STA	04	Store A	MR	1.92	2-3
STX	15	Store X	MR	1.92	2-3

APPENDIX C (Cont)
SUMMARY OF STANDARD INSTRUCTIONS
(Listed in Alphabetical Order)

Mnemonic	Octal Code	Instruction	Type	Execution Time (μsec)	Page
SUB	07	Subtract	MR	1.92	2-4
SZE	100040	Skip if A ZERO	G	0.96	2-12
TCA	140407	Two's Complement A	G	1.44	2-4

APPENDIX D
SUMMARY OF STANDARD INSTRUCTIONS (LISTED IN NUMERICAL ORDER)

Octal Code	Mnemonic	Instruction	Type	Execution Time (μsec)	Page
01	JMP	Unconditional Jump	MR	0.96	2-11
02	LDA	Load A	MR	1.92	2-3
03	ANA	AND to A	MR	1.92	2-4
04	STA	Store A	MR	1.92	2-3
05	ERA	Exclusive OR to A	MR	1.92	2-4
06	ADD	Add	MR	1.92	2-3
07	SUB	Subtract	MR	1.92	2-4
10	JST	Jump and Store Location	MR	2.88	2-11
11	CAS	Compare	MR	2.88	2-10
12	IRS	Increment, Replace & Ship	MR	2.88	2-11
13	IMA	Interchange Memory and A	MR	2.88	2-3
14	OCP	Output Control Pulse	IO	1.92	2-9
15	LDX*	Load X	MR	2.88	2-3
15	STX*	Store X	MR	1.92	2-3
34	SKS	Skip if Ready Line Set	IO	1.32	2-10
54	INA	Input to A	IO	1.92	2-9
74	OTA**	Output from A	IO	1.92	2-9
74	SMK**	Set Mask	IO	1.92	2-10
0400	LRL	Long Rght Logical Shift	SH	0.96+0.48N	2-7
0401	LRS	Long Arithmetic Right Shift	SH	0.96+0.48N	2-8
0402	LRR	Long Right Rotate	SH	0.96+0.48N	2-8
0404	LGR	Logical Right Shift	SH	0.96+0.48N	2-5
0405	ARS	Arithmetic Right Shift	SH	0.96+0.48N	2-5
0406	ARR	Logical Right Rotate	SH	0.96+0.48N	2-5
0410	LLL	Long Left Logical Shift	SH	0.96+0.48N	2-6
0411	LLS	Long Arithmetic Left Shift	SH	0.96+0.48N	2-7
0412	LLR	Long Left Rotate	SH	0.96+0.48N	2-6
0414	LGL	Logical Left Shift	SH	0.96+0.48N	2-5
0415	ALS	Arithmetic Left Shift	SH	0.96+0.48N	2-4
0416	ALR	Logical Left Rotate	SH	0.96+0.48N	2-4
000000	HLT	Halt	G	1.44	2-10
000043	INK	Input Keys	G	0.96	2-3
000201	IAB	Interchange A and B	G	0.96	2-3
000401	ENB	Enable Program Interrupt	G	0.96	2-10
001001	INH	Inhibit Program Interrupt	G	0.96	2-10
100000	SKP	Unconditional Skip	G	0.96	2-11
100001	SRC	Skip if C Reset	G	0.96	2-12
100002	SR4	Skip if Sense Switch No. 4 Reset	G	0.96	2-12
100004	SR3	Skip if Sense Switch No. 3 Reset	G	0.96	2-11
100010	SR2	Skip if Sense Switch No. 2 Reset	G	0.96	2-11
100020	SR1	Skip if Sense Switch No. 1 Reset	G	0.96	2-11
100036	SSR	Skip if No Sense Switch Set	G	0.96	2-12
100040	SZE	Skip if A Zero	G	0.96	2-12
100100	SLZ	Skip if(A_{16}) is Zero	G	0.96	2-11
100400	SPL	Skip if A Sign Plus	G	0.96	2-11
101000	NOP	No Operation	G	0.96	2-11
101001	SSC	Skip if C Bill Set	G	0.96	2-12
101002	SS4	Skip if Sense Switch No. 4 Set	G	0.96	2-12
101004	SS3	Skip if Sense Switch No. 3 is Set	G	0.96	2-12

Octal Code	Mnemonic	Instruction	Type	Execution Time (μsec)	Page
101010	SS2	Skip if Sense Switch No. 2 Set	G	0.96	2-12
101002	SS1	Skip if Sense Switch No. 1 Set	G	0.96	2-12
101036	SSS	Skip if Any Sense Switch Set	G	0.96	2-12
101040	SNZ	Skip if A Non-Zero	G	0.96	2-11
101100	SLN	Skip if (A_{16}) is One	G	0.96	2-11
101400	SMI	Skip if A Sign Minus	G	0.96	2-11
140024	CHS	Complement ASign	G	0.96	2-4
140040	CRA	Clear A	G	0.96	2-3
140100	SSP	Set A Sign Plus	G	0.96	2-4
140200	RCB	Reset C Bit	G	0.96	2-11
140320	CSA	Copy Sign and Set Sign Plus	G	0.96	2-4
140401	CMA	Complement A	G	0.96	2-4
140407	TCA	Z's Complement A	G	1.44	2-4
140500	SSM	Set A Sign Minus	G	0.96	2-4
140600	SCB	Set C Bit	G	0.96	2-11
141044	CAR	Clear A, Right Half	G	0.96	2-12
141050	CAL	Clear A, Left Half	G	0.96	2-12
141140	ICL	Interchange and Clear Left Half of A	G	0.96	2-13
141206	AOA	Add One to A	G	0.96	2-3
141216	ACA	Add C to A	G	0.96	2-3
141240	ICR	Interchange and Clear Right Half of A	G	0.96	2-13
141340	ICA	Interchange Characters in A	G	0.96	2-12
171020	OTK	Output Keys	G	1.92	2-3

N=Number of shifts

*Instructions STX and LDX have the same operation code (15). STX has an index bit of 0; LDX has an index bit of 1

**Instructions OTA and SMK have the same operations code (74). SMK has device address D=20 or 24; OTA has D≠20 or 24.

APPENDIX E
MAIN FRAME OPTION COMMANDS

Mnemonic	Octal Code	Instruction	Type	Execution Time	Page
Extended Addressing for 24K and 32K Memories - Model 516-05, 06					
DXA	000011	Disable Extended Mode	G	0.96	4-5
EXA	000013	Enable Extended Mode	G	0.96	4-5
Memory Parity - Model 516-07					
RMP	000021	Reset Memory Parity Error	G	0.96	4-7
SMK '0020	170020	Set Interrupt Mask (A_{15})	IO	1.92	4-7
SPN	100200	Skip if No Memory Parity Error	G	0.96	4-7
SPS	101200	Skip if Memory Parity Error	G	0.96	4-7
Memory Lockout - Model 516-08					
ERM	001401	Enter Restricted Mode	G	0.96	4-13
SMK '1320	171320	Set Relocation Register	IO	1.92	4-13
SMK '1420	171420	Set Lockout Mask 1	IO	1.92	4-13
SMK '1520	171520	Set Lockout Mask 2	IO	1.92	4-13
SMK '1620	171620	Set Lockout Mask 3	IO	1.92	4-13
SMK '1720	171720	Set Lockout Mask 4	IO	1.92	4-13
Direct Memory Access (DMA) - Model 516-21					
INA '1124	171124	Read Range Counter Channel 1	IO	1.92	4-25
INA '1224	171224	Read Range Counter Channel 2	IO	1.92	4-25
INA '1324	171324	Read Range Counter Channel 3	IO	1.92	4-25
INA '1424	171424	Read Range Counter Channel 4	IO	1.92	4-25
SMK '0124	170124	Load Address Counter Channel 1	IO	1.92	4-24
SMK '0224	170224	Load Address Counter Channel 2	IO	1.92	4-24
SMK '0324	170324	Load Address Counter Channel 3	IO	1.92	4-24
SMK '0424	170424	Load Address Counter Channel 4	IO	1.92	4-24
SMK '1124	171124	Load Range Counter Channel 1	IO	1.92	4-24
SMK '1224	171224	Load Range Counter Channel 2	IO	1.92	4-24
SMK '1324	171324	Load Range Counter Channel 3	IO	1.92	4-25
SMK '1424	171424	Load Range Counter Channel 4	IO	1.92	4-25

Mnemonic	Octal Code	Instruction	Type	Execution Time	Page
Priority Interrupt - Model 516-25					
SMK '0020	170020	Set Standard Interrupt Mask	IO	1.92	4-27
SMK '0120	170120	Set Interrupt Mask Lines 1-16	IO	1.92	4-27
SMK '0220	170220	Set Interrupt Mask Lines 17-32	IO	1.92	4-27
SMK '0320	170320	Set Interrupt Mask Lines 33-48	IO	1.92	4-27
High-Speed Arithmetic Unit - Model 516-11					
DAD	06	Double Precision Add	MR	2.88	4-16
DBL	000007	Enter Double Precision Mode	G	0.96	4-16
DIV	17	Divide	MR	10.56 (max)	4-16
DLD	02	Double Precision Load	MR	2.88	4-16
DSB	07	Double Precision Subtract	MR	2.88	4-16
DST	04	Double Precision Store	MR	2.88	4-16
MPY	16	Multiply	MR	5.28	4-16
NRM	000101	Normalize	G	0.96+0.48n	4-16
SCA	000041	Shift Count to A	G	0.96	4-16
SGL	00005	Enter Single Precision Mode	G	0.96	4-16
Real-Time Clock - Model 516-12					
OCP '0220	030220	Reset Interrupt Request and Stop Clock	IO	1.92	4-17
OCP '0020	030020	Reset Interrupt Request and Run Clock	IO	1.92	4-17
SKS '0020	070020	Skip if RTC not interrupting	IO	1.92	4-17
SMK '0020	070020	Set Interrupt Mask (A_{16})	IO	1.92	4-17

APPENDIX F
PERIPHERAL DEVICE COMMANDS

ASR 33/35 Model 516-53/55

OCP	0004	Enable ASR-33/35 In Input Mode
OCP	0104	Enable ASR-33/35 In Output Mode
SKS	0004	Skip if ASR-33/35 is Ready
SKS	0104	Skip if ASR-33/35 is Not Busy
SKS	0404	Skip if ASR-33/35 is Not Interrupting
SKS	0504	Skip if Stop Code Was Not Read on ASR-33/35
INA	0004	Input in ASCII from ASR-33/35
INA	0204	Input in Binary from ASR-33/35
INA	1004	Clear Register A and Input in ASCII from ASR-33/35
INA	1204	Clear Register A and Input in Binary from ASR-33/35
OTA	0004	Output in ASCII to ASR-33/35
OTA	0204	Output in Binary to ASR-33/35
SMK	0020	Set Interrupt Mask (A_{11})

High Speed Paper Tape Reader - Model 516-50

OCP	0001	Start Paper Tape Reader
OCP	0101	Stop Paper Tape Reader
SKS	0001	Skip if Paper Tape Reader is Ready
SKS	0401	Skip if Paper Tape Reader is Not Interrupting
INA	0001	Input from Paper Tape Reader
INA	1001	Clear Register A and Input From Paper Tape Reader
SMK	0020	Set Interrupt Mask (A_9)

High Speed Paper Tape Punch - Model 516-52

OCP	0002	Enable Paper Tape Punch
OCP	0102	Turn Paper Tape Punch Power Off
SKS	0002	Skip if Paper Tape Punch is Ready
SKS	0102	Skip if Paper Tape Punch is Enabled
SKS	0402	Skip if Paper Tape Punch is Not Interrupting
OTA	0002	Output To Paper Tape Punch
SMK	0020	Set Interrupt Mask (A_{10})

Parallel Channels - Model 516-32, 33-34

INA	'0030*	Input to A-register
INA	'1030	Clear A-register and input to A-register
OTA	'0030	Output from A-register
OCP	'0030	Enable input mode (516-32, 34)
OCP	'0030	Enable output mode (516-33)

OCP	'0130	Enable output mode (516-34)
OCP	'0130	Device OCP 1 (516-32-33)
OCP	'0230	Device OCP 2 (516-32, 33, 34)
OCP	'0330	Device OCP 3 (516-32, 33, 34)
OCP	'0430	Device OCP 4 (516-33, 34)
OCP	'0530	Device OCP 5 (516-34)
OCP	'0630	Device OCP 6 (516-34 No DMC/DMA)
OCP	'0630	Enable DMC/DMA mode (516-32, 33, 34)
OCP	'0730	Reset DMC/DMA mode (516-32, 33, 34)
OCP	'1630	Enable DMC/DMA Auto-Switch Mode (516-32, 33, 34)
SKS	'0030	Skip if channel ready
SKS	'0130	Device SKS 1
SKS	'0230	Skip if first channel not reached end-of-range
SKS	'0330	Skip if not in auto-switch mode
SKS	'0430	Skip if no interrupt request
SKS	'0530	Device SKS 2
SKS	'0630	Device SKS 3
SMK	'0020	

*30 is the address of the 1st channel. Table below shows addresses for two other channels.

	Address	Mask Bit
First Channel	30_8	5
Second Channel	31_8	6
Third Channel	32_8	7

OCP/SKS - Model 516-29

OCP	'0034	Device OCP 00
OCP	'0134	Device OCP 01
OCP	'0234	Device OCP 02
OCP	'0334	Device OCP 03
OCP	'0434	Device OCP 04
OCP	'0534	Device OCP 05
OCP	'0634	Device OCP 06
OCP	'0734	Device OCP 07
OCP	'1034	Device OCP 10
OCP	'1134	Device OCP 11
OCP	'1234	Device OCP 12
OCP	'1334	Device OCP 13
OCP	'1434	Device OCP 14
OCP	'1534	Device OCP 15

OCP	'1634	Device OCP 16
OCP	'1734	Device OCP 17
SKS	'0034	Device SKS 00
SKS	'0134	Device SKS 01
SKS	'0234	Device SKS 02
SKS	'0334	Device SKS 03
SKS	'0434	Device SKS 04
SKS	'0534	Device SKS 05
SKS	'0634	Device SKS 06
SKS	'0734	Device SKS 07
SKS	'1034	Device SKS 10
SKS	'1134	Device SKS 11
SKS	'1234	Device SKS 12
SKS	'1334	Device SKS 13
SKS	'1434	Device SKS 14
SKS	'1534	Device SKS 15
SKS	'1634	Device SKS 16
SKS	'1734	Device SKS 17

Card Reader - Model 516-61

OCP	'0005	Read One Hollerith Card
OCP	'0105	Read One Binary Card
SKS	'0005	Skip if Card Reader Ready
SKS	'0105	Skip if Card Reader Not Busy
SKS	'0205	Skip if Not End of File
SKS	'0305	Skip if Card Reader Operational
SKS	'0405	Skip if Card Reader Not Interrupting
INA	'0005	Input From Card Reader if Ready
INA	'1005	Clear A-Register and Input From Card Reader if Ready
SMK	'0020	Set Interrupt Mask (A_{12})

Line Printer - Model 516-7050

OCP	'0003	No paper advance
OCP	'0203	Advance paper to channel 2
OCP	'0303	Allow memory scan via DMA/DMC
OCP	'0403	Advance paper to channel 1
OCP	'0703	Allow memory scan via the I/O Bus
SKS	'0003	Skip if ready
SKS	'0203	Skip if no alarm
SKS	'0303	Skip if odd column next
SKS	'0403	Skip if not interrupting
SKS	'1103	Skip if line is printed

SKS	'1203	Skip if not shuttling
SKS	'1303	Skip if line is printed and not shuttling
SKS	'1403	Skip if not advancing paper
SKS	'1503	Skip if line is printed and not advancing paper
SKS	'1603	Skip if not shuttling and not advancing paper
SKS	'1703	Skip if not busy
OTA	'0003	Output to line printer if ready
SMK	'0020	Set Interrupt Mask (A_{14})

Magnetic Tape Systems - Model 516-4100

OCP	1001X	Read BCD, 2 char/word
OCP	'011X	Read binary, 2 char/word
OCP	'021X	Read binary, 3 char/word
OCP	'031X	Set up Normal DMC/DMA mode
OCP	'041X	Write BCD, 2 char/word
OCP	'051X	Write binary, 3 char/word
OCP	'061X	Write end of file
OCP	'071X	Reset DMC/DMA mode
OCP	'101X	Write binary, 3 char/word
OCP	'111X	Space forward one space
OCP	'121X	Space forward one file
OCP	'131X	Set up DMC/DMA in Auto Switch mode
OCP	'141X	Rewind
OCP	'151X	Backspace one record
OCP	'161X	Backspace one file
OCP	'171X	Stop write
SKS	'001X	Skip if ready
SKS	'011X	Skip if not busy
SKS	'021X	Skip if an error has not been detected
SKS	'031X	Skip if not at beginning of tape (loadpoint)
SKS	'041X	Skip if not interrupting
SKS	'051X	Skip if end of tape has not been detected
SKS	'061X	Skip if end of file has not been detected
SKS	'071X	Skip if writing is permitted
SKS	'111X	Skip if MTT operational
SKS	'121X	Skip if DMA/DMC Sub-channel is not currently processing Channel #2
SKS	'131X	Skip if DMC/DMA Sub-channel is not in Auto Switch mode
SKS	'141X	Skip if not rewinding
INA	'001X	Input from TCU if ready
INA	'101X	Clear A-register and input from TCU if ready
OTA	'001X	Output data to the TCU
SMK	'0020	Set TCU Interrupt Mode, (A_1) for TCU #1, (A_2) for TCU #2

Fixed Head Disc File - Model 516-4400

INA	'0022	Input to A-register
INA	'1022	Clear A-register and Input to A-register
OTA	'0022	Output from A-register
OCP	'0322	Select DMA or DMC operation
OCP	'0422	Stop data transfer/acknowledge interrupt
OCP	'0722	Select I/O bus operation
SKS	'0022	Skip if Fixed Head Disc File ready
SKS	'0122	Skip if Fixed Head Disc File is not busy
SKS	'0222	Skip if Fixed Head Disc File has not detected a data transfer error
SKS	'0322	Skip if Fixed Head Disc File has not detected an access error
SKS	'0422	Skip if Fixed Head Disc File is not interrupting
SMK	'0020	Set Interrupt Mask (A_8)

Moving Head Disc File - Model 516-4600

INA	'1025	Clear A-register and input to A-register
INA	'0025	Input to A-register
OTA	'0025	Output from A-register
OCP	'0025	Return to zero seek
OCP	'0125	Direct seek
OCP	'0225	Read current address
OCP	'0325	Enable DMC/DMA mode of data transfer
OCP	'0525	Write track format
OCP	'0625	Read/write record
OCP	'0725	Enable I/O bus mode of data transfer
OCP	'1025	Stop transfer
OCP	'1425	Acknowledge interrupt
SKS	'0025	Skip if ready
SKS	'0125	Skip if not busy
SKS	'0225	Skip if data error not detected
SKS	'0325	Skip if set up error not detected
SKS	'0425	Skip if not interrupting
SKS	'1425	Skip if unit 1 not seeking
SKS	'1525	Skip if unit 2 not seeking
SKS	'1625	Skip if unit 3 not seeking
SKS	'1725	Skip if unit 4 not seeking
SMK	'0020	Set interrupt mask (A_4)

Process Interface Controller - Model 516-8100 Series

OCP	'XX33	Acknowledge designated subsystem interrupt
SKS	'0023	Skip if PIC is ready
SKS	'0033	Skip if PIC is not interrupting
SKS	'XX33	Skip if designated subsystem is not interrupting
INA	'0023	Input from PIC Adapter if ready
INA	'1023	Clear Register A and input from PIC Adapter if ready
OTA	'0123	Output select to PIC if ready
OTA	'0323	Output data to PIC if ready
OTA	'0723	Output and cycle PIC if ready
OTA	'1033	Set PIC interrupt mask

Single Line Controller

OCP	'0060*	Enable receiver
OCP	'0160	Receive sync (synchronous controller only)
OCP	'0260	Enable transmitter
OCP	'0360	Set data terminal ready
OCP	'0460	Originate call
OCP	'0560	Enable DMC receive mode
OCP	'0660	Enable DMC transmit mode
OCP	'0760	Enable low speed receiver
OCP	'1060	Disable receiver
OCP	'1160	Transmit break (asynchronous controller only)
OCP	'1260	Disable transmitter
OCP	'1360	Reset data terminal ready
OCP	'1560	Disable DMC transmit mode
OCP	'1760	Enable low speed transmitter
SKS	'0060	Skip if receiver ready
SKS	'0160	Skip if receiver fault is set
SKS	'0260	Skip if transmitter ready
SKS	'0360	Skip if no ring signal
SKS	'0460	Skip if controller not interrupting
SKS	'0560	Skip if receiver ERL signal
SKS	'0660	Skip if transmitter ERL signal
SKS	'1060	Skip if receiver ready
SKS	'1260	Skip if transmitter not busy (synchronous controller only)
SKS	'1360	Skip if no disconnect signal
SKS	'1460	Skip if no abandon call and retry signal
OTA	'0160	Skip if receiver fault is set and reset it
OTA	'0260	Transmit character

*'60 is address of first channel.

```
INA     '0060     Input character
INA     '1060     Clear A-register and input character
SMK     '0420
```

Table below shows addresses of the first four channels and mask bit assignments.

	Address	Mask Bit
Single line controller 1	$60_{(8)}$	1
Single line controller 2	$61_{(8)}$	2
Single line controller 3	$62_{(8)}$	3
Single line controller 4	$63_{(8)}$	4

APPENDIX G
DEDICATED LOCATIONS

Octal Address	Assignment
00000	Index Register
00001 thru 00017	Protected Fill Program
00020	Starting Addresses DMC Channel 1
00021	Final Addresses DMC Channel 1
00022 thru 00057	DMC Channels 2 thru 16
00060	Power Failure Interrupt Link
00061	Real-Time Clock
00062	Location Violation Int. Link
00063	Standard Interrupt Link
00064	Optional PI No. 1 Link
00065 thru 00143	Optional PI No. 2 thru 48 Links

APPENDIX H
KEY-IN LOADER

Key-In Loader for ASR-33/35/High-Speed Paper Tape Reader

```
*    TO LOAD PAL-MODE PROGRAMS, THE FOLLOWING PROCEDURE
*    MUST BE FOLLOWED.
*      1.  IF THE KEY-IN LOADER IS NOT PRESENT IN LOCATIONS
*          1-17 OCTAL, MANUALLY KEY IN THE FOLLOWING:
*                                              ASR       DIGITRONICS
*              1 STA    '57                   010057    010057
*              2 OCP    '0001/4               030004    030001
*              3 INA    '1001/4               131004    131001
*              4 JMP    *-1                   002003    002003
*              5 SNZ                          101040    101040
*              6 JMP    *-3                   002003    002003
*              7 STA    0                     010000    010000
*              10 INA    '1001/4              131004    131001
*              11 JMP    *-1                  002010    002010
*              12 LGL    8                    041470    041470
*              13 INA    '0001/4              130004    130001
*              14 JMP    *-1                  002013    002013
*              15 STA*    0                   110000    110000
*              16 IRS    0                    024000    024000
*              17 SZE                         100040    100040
*
*      2.  MASTER CLEAR
*      3.  SET P REGISTER TO 1
*      4.  MOUNT PAL-MODE TAPE IN INPUT DEVICE AND PRESS START
```